Commercial Grade
-220S series
CFast Card

Product Manual

May 29, 2014

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1.Introduction to Cactus Technologies® Commercial Grade -220S Series CFast Products

Features:

- Solid state design with no moving parts
- Industry standard CFast Type I form factor
- Capacities from 4GB to 128GB
- Compliant with Serial ATA 2.6 specifications
- ATA-8 compatible and CFast 1.0 compliant
- Supports Serial ATA Generation I/II transfer rate of 1.5/3.0Gbps
- Support ATA SMART Feature Set
- Support ATA Security Feature Set
- ECC capable of correcting up to 72 bit errors per 1KB
- Enhanced error correction, < 1 error in 10^{14} bits read
- SATA partial and slumber modes and CFast PHYSLP mode supported
- Voltage support: 3.3V±10%

Cactus Technologies® CFast card is a high capacity solid-state flash memory product that complies with the Serial ATA 2.6 standard and is functionally compatible with a SATA hard disk drive. Cactus Technologies® CFast cards provide up to 128GB of formatted storage capacity.

Cactus Technologies® CFast product uses high quality MLC NAND flash memory from well known vendors, such as Micron Corporation. In addition, it include an on-drive intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control. The controller's firmware is upgradeable, thus allowing feature enhancements and firmware updates while keeping the BOM stable.

1.1. Supported Standards

Cactus Technologies® CFast card is fully compatible with the following specification:

- ATA 8 Specification published by ANSI
- Serial ATA 2.6 Specification published by the Serial ATA International Organization
- CFast 1.0 Specification published by CFA

1.2. Product Features

Cactus Technologies® Commercial CFast card contains a high level, intelligent controller. This intelligent controller provides many capabilities including the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

1.2.1. Host and Technology Independence

Cactus Technologies® Commercial CFast card appears as a standard SATA disk drive to the host system. The drive utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the drive as per the SATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the drive. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support the Cactus Technologies® Commercial CFast products today will continue to work with future Cactus Technologies® Commercial CFast cards built with new flash technology without having to update or change host software.

1.2.2. Defect and Error Management

Cactus Technologies® Commercial CFast card contains a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies® Commercial CFast card is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the drive has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies® Commercial CFast cards unparalleled reliability.

1.2.3. Power Supply Requirements

Cactus Technologies® Commercial CFast card operates at a voltage range of 3.3 volts ± 10%.

2.Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. Environmental Specifications

		Cactus Technologies® Commercial CFast
Temperature	Operating:	0° C to +70° C (Standard)
Humidity	Operating & Non-Operating:	8% to 95%, non-condensing
Vibration	Operating & Non-Operating:	20G, MIL-STD-883G Method 2005.2, Condition A
Shock	Operating & Non-Operating:	3,000 G, MIL-STD-883G Method 2002.4, Condition C
Altitude (relative to sea level)	Operating & Non-Operating:	100,000 feet maximum

2.2. System Power Requirements

Table 2-2. Power Requirements

		Cactus Technologies® Commercial CFast
DC Input Voltage (VCC) 100 mV max. ripple (p-p)		3.3V ±10%
(Maximum Average Value) See Notes.	Sleep: Reading: Writing:	70 mA 215 mA 320 mA

NOTES: All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all drive inputs are static CMOS levels and in a “Not Busy“ operating state.

2.3. System Performance

All performance timings assume the drive controller is in the default (i.e., fastest) mode.

Table 2-3. Performance

Start Up Times	Reset to ready:	35 msec typical
Read Transfer Rate	4-8GB 16GB 32GB 64-128GB	Up to 35MBytes/sec Up to 70MBytes/sec Up to 135MBytes/sec Up to 170MBytes/sec
Write Transfer Rate	4-8GB 16GB 32GB 64-128GB	Up to 10 Mbytes/sec Up to 20 Mbytes/sec Up to 40 Mbytes/sec Up to 75MBytes/sec

.

2.4. System Reliability

Table 2-4. Reliability

Data Reliability	< 1 non-recoverable error in 10^{14} bits READ
Endurance:	> 100,000 erase/program cycles per logical sector

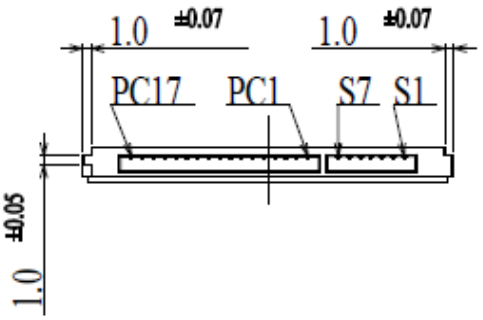
2.5. Physical Specifications

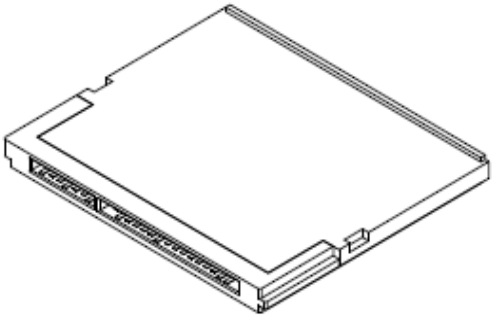
The following sections provide the physical specifications for Cactus Technologies® Commercial CFast products.

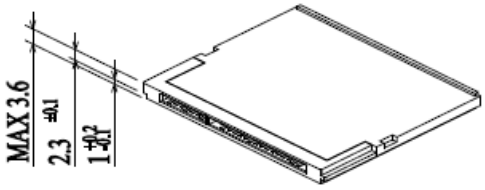
2.5.1. CFast Card Physical Specifications

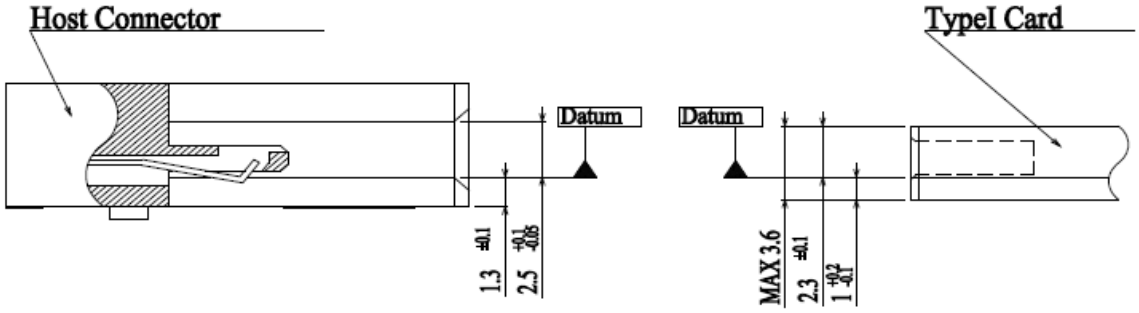
Table 1: Type I CFast Card Physical Specifications

Length:	36.4 ± 0.15 mm (1.433 ±.006 in.)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in.)
Thickness Including Label Area:	3.6 mm maximum (.1418 in maximum).









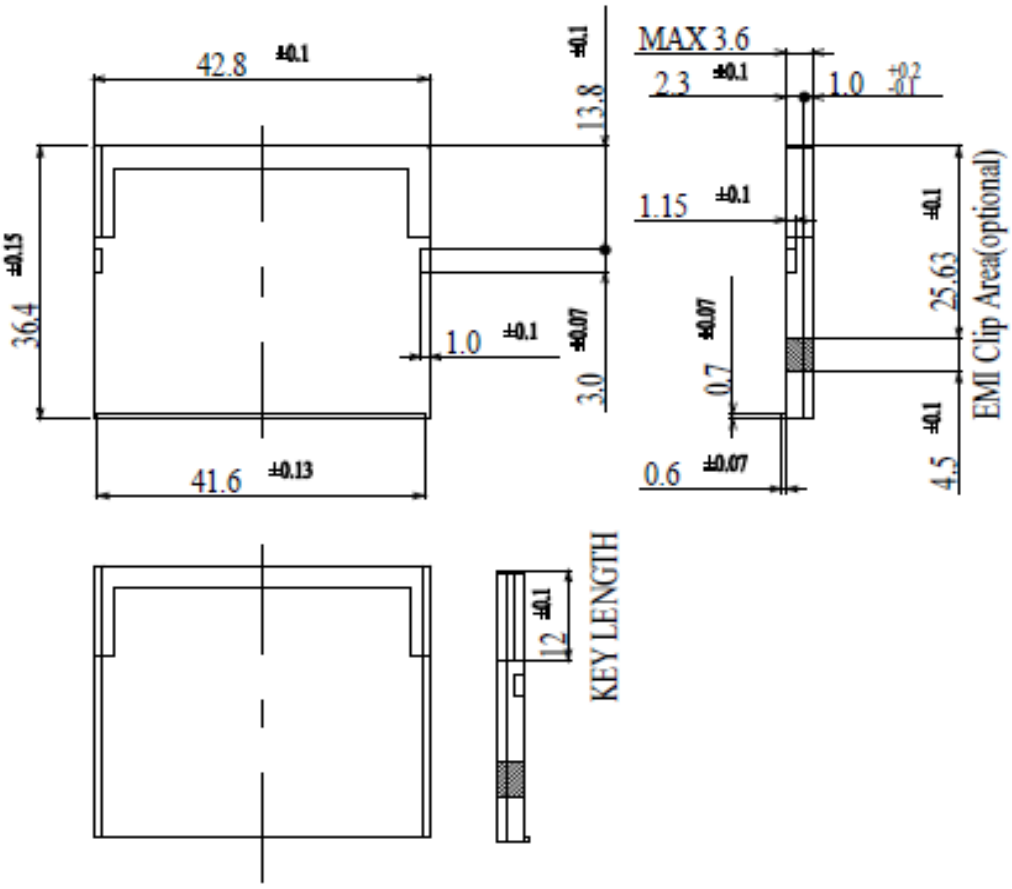


Figure 2-1. Type I CFast Card Dimensions

3.Interface Description

The following sections provide detailed information on the Cactus Technologies® Commercial CFast card interface.

3.1. CFast Pin Assignments and Pin Type

Cactus Technologies® CFast signal pinout conforms to CFA specifications. The signal/pin assignments and descriptions are listed in Table 3-5.

Table 3-5. CFast Pin Assignments and Pin Type

Number	Segment	Name	Type	Description	Mate Sequence
S1	SATA	SGND	Signal GND	Ground for signal integrity	1st
S2	SATA	A+	SATA Differential	Signal Pair A	2nd
S3	SATA	A-	SATA Differential		2nd
S4	SATA	SGND	Signal GND	Ground for signal integrity	1st
S5	SATA	B-	SATA Differential	Signal Pair B	2nd
S6	SATA	B+	SATA Differential		2nd
S7	SATA	SGND	Signal GND	Ground for signal integrity	1st
	Key				
	Key				
PC1	PWR/CTL	CDI	CMOS Input	Card Detect In	3rd
PC2	PWR/CTL	GND	Device GND		1st
PC3	PWR/CTL	TBD	TBD		2nd
PC4	PWR/CTL	TBD	TBD		2nd
PC5	PWR/CTL	TBD	TBD		2nd
PC6	PWR/CTL	TBD	TBD		2nd
PC7	PWR/CTL	GND	Device GND		1st
PC8	PWR/CTL	LED1	LED Output	LED Output	2nd
PC9	PWR/CTL	LED2	LED Output	LED Output	2nd
PC10	PWR/CTL	IO1	CMOS Input/Output	Reserved Input/Output	2nd
PC11	PWR/CTL	IO2	CMOS Input/Output	Reserved Input/Output	2nd
PC12	PWR/CTL	IO3	CMOS Input/Output	Reserved Input/Output	2nd
PC13	PWR/CTL	PWR	3.3V	Device Power (3.3V)	2nd
PC14	PWR/CTL	PWR	3.3V	Device Power (3.3V)	2nd
PC15	PWR/CTL	PGND	Device GND	Device Ground	1st
PC16	PWR/CTL	PGND	Device GND	Device Ground	1st
PC17	PWR/CTL	CDO	CMOS Output	Card Detect Out	3rd

3.2. Electrical Specifications

The following table defines all D.C. Characteristics for the CFast products. Unless otherwise stated, conditions are:

Vcc = 3.3V ± 10%
Ta = 0°C to 70°C

3.2.1. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Storage Temperature	Ts	-40	+85	°C
Operating Temperature	T_A	0	+70	°C
Vcc with respect to GND	Vcc	-0.3	3.6	V

3.2.2. DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	Vin	-0.5	Vcc + 0.5	V
Output Voltage	Vout	-0.3	Vcc + 0.3	V
Input Leakage Current	I_{LI}	-10	10	uA
Output Leakage Current	I_{LO}	-10	10	uA
Input/Output Capacitance	C_I/C_o		10	pF
Operating Current	I_{CC}			mA
Sleep Mode			70	
Active			320	

3.2.3. AC Characteristics

Cactus Technologies® CFast products conforms to all AC timing requirements as specified in the CFA specifications. Please refer to that document for details of AC timing for all operation modes of the device.

4.ATA Drive Register Set Definition and Protocol

The communication to or from the CFast card is done using FIS. Legacy ATA protocol is supported by using the legacy mode defined in the SATA specifications. In this mode, the FIS has defined fields which provide all the necessary ATA task file registers for control and status information. The Serial ATA interface does not support Primary/Secondary or Master/Slave configurations. Each SATA channel supports only one SATA device, with the register selection as defined by the ATA standard.

4.1. ATA Task File Definitions

The following sections describes the usage of the ATA task file registers. Note that the Alternate Status Register of legacy ATA is not defined for SATA drives.

4.1.1. Data Register

The Data Register is a 16-bit register, and it is used to transfer data blocks between the SSD data buffer and the Host.

4.1.2. Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

4.1.3. Feature Register

This register provides information regarding features of the SSD that the host can utilize.

4.1.4. Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the SSD. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

4.1.5. Sector Number (LBA 7-0) Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any SSD data access for the subsequent command.

4.1.6. Cylinder Low (LBA 15-8) Register

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

4.1.7. Cylinder High (LBA 23-16) Register

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

4.1.8. Drive/Head (LBA 27-24) Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.
Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.
Bit 5 This bit is set to 1.
Bit 4 (DRV) DRV is the drive number. This should always be set to 0.
Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

4.1.9. Status Registers

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the device has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the device is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the device is ready.

Bit 3 (DRQ) The Data Request is set when the device requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

4.1.10. Device Control Register

This register is used to control the drive interrupt request and to issue an ATA soft reset to the drive. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
HOB	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is used in 48-bit addressing mode. When cleared, the host can read the most recently written values of the Sector Count,Drive/Head and LBA registers. When set, the host will read the previous written values of these registers. A write to any Command block register will clear this bit.

Bit 6 This bit is an X (Do not care).

Bit 5 This bit is an X (Do not care).

Bit 4 This bit is an X (Do not care).

Bit 3 This bit is ignored by the drive.

Bit 2 (SW Rst) This bit is set to 1 in order to force the drive to perform an AT Disk controller Soft Reset operation. The drive remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the drive are disabled. This bit is set to 0 at power on and Reset.

Bit 0 This bit is ignored by the drive.

4.1.11. Drive Address Register

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.
Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the SSD. Following are some possible solutions to this problem:

1. Locate the SSD at a non-conflicting address (i.e., Secondary address (377) when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and a SSD in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a SSD product is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the SSD's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the SSD or b) if provided use an additional Primary/Secondary configuration in the SSD that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

5.ATA Command Description

This section defines the ATA command set supported by the Cactus Technologies® CFast card.

5.1. ATA Command Set

Table 5-6 summarizes the supported ATA command set .

Table 5-6. ATA Command Set

COMMAND	Code	FR	SC	SN	CY	DH
Check Power Mode	E5h, 98h	-	-	-	-	D
Erase Sector(s)	C0h	-	Y	Y	Y	D
Execute Drive Diagnostic	90h	-	-	-	-	-
Flush Cache	E7h	-	-	-	-	D
Flush Cache Ext	EAh	-	-	-	-	D
Identify Drive	ECh	-	-	-	-	D
Idle	E3h, 97h	-	Y	-	-	D
Idle Immediate	E1h, 95h	-	-	-	-	D
Initialize Drive Parameters	91h	-	-	-	-	D
NOP	00h	-	-	-	-	D
Read Buffer	E4h	-	-	-	-	D
Read DMA	C8h	-	Y	Y	Y	Y
Read DMA Ext	25h	-	Y	Y	Y	D
Read Multiple	C4h	-	Y	Y	Y	Y
Read Multiple Ext	29h	-	Y	Y	Y	D
Read Native Max Address	F8h	-	-	-	-	D
Read Native Max Address Ext	27h	-	-	-	-	D
Read Sector(s)	20h, 21h	-	Y	Y	Y	Y
Read Sector(s) Ext	24h	-	Y	Y	Y	D

COMMAND	Code	FR	SC	SN	CY	DH
Read Verify Sector(s)	40h, 41h	-	Y	Y	Y	Y
Read Verify Sector(s) Ext	42h	-	Y	Y	Y	D
Request Sense	03h	-	-	-	-	D
Security Disable Password	F6h	-	-	-	-	D
Security Erase Prepare	F3h	-	-	-	-	D
Security Erase Unit	F4h	-	-	-	-	D
Security Freeze Lock	F5h	-	-	-	-	D
Security Set Password	F1h	-	-	-	-	D
Security Unlock	F2h	-	-	-	-	D
Seek	70h	-	-	Y	Y	Y
Set Features	EFh	Y	-	-	-	D
Set Max Address	F9h	-	Y	Y	Y	Y
Set Max Address Ext	37h	-	Y	Y	Y	D
Set Multiple Mode	C6h	-	Y	-	-	D
Set Sleep Mode	E6h, 99h	-	-	-	-	D
SMART	B0h	Y	Y	-	Y	D
Stand By	E2h, 96h	-	-	-	-	D
Stand By Immediate	E0h, 94h	-	-	-	-	D
Translate Sector	87h	-	-	Y	-	D
Wear Level	F5h	-	-	-	-	D
Write Buffer	E8h	-	-	-	-	D
Write DMA	Cah, CBh	-	Y	Y	Y	Y
Write DMA Ext	35h	-	Y	Y	Y	D
Write DMA FUA Ext	3Dh	-	Y	Y	Y	D
Write Multiple	C5h	-	Y	Y	Y	Y
Write Multiple Ext	39h	-	Y	Y	Y	D
Write Multiple FUA Ext	CEh	-	Y	Y	Y	D
Write Multiple Without Erase	CDh	-	Y	Y	Y	D
Write Sector(s)	30h, 31h	-	Y	Y	Y	Y
Write Sector(s) Ext	34h	-	Y	Y	Y	D
Write Sector(s) Without Erase	38h	-	Y	Y	Y	D

Definitions: FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Drive/Drive/Head Register.
Y—The register contains a valid parameter for this command. For the Drive/Head Register Y means both the drive and head parameters are used; D—only the drive parameter is valid and not the head parameter.

Note: 1. For SATA drives, the drive number is always 0.

5.1.1. Identify Drive—ECH

The Identify Drive command enables the host to receive parameter information from the drive. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 5-7. All reserved bits or words are zero. Table 5-7 is the definition for each field in the Identify Drive Information.

Table 5-7. Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit-significant information.
1	XXXXH	2	Default number of cylinders; capacity dependent.
2	0000H	2	Reserved.

Word Address	Default Value	Total Bytes	Data Field Type Information
3	00XXH	2	Default number of heads; capacity dependent.
4	0000H	2	Number of unformatted bytes per track.
5	0240H	2	Number of unformatted bytes per sector.
6	XXXXH	2	Default number of sectors per track; capacity dependent.
7-8	XXXXH,XXXXH	4	Number of sectors per drive (Word 7 = MSW, Word 8 = LSW); capacity dependent.
9	0000H	2	Reserved.
10-19	aaaa	20	Serial number in ASCII (Right Justified).
20	0002H	2	Buffer type (dual ported multi-sector)
21	0002H	2	Buffer size in 512 bytes increments
22	0004H	2	# of ECC bytes passed in R/W Long commands
23-26	aaaa	8	Firmware revision in ASCII . Big Endian Byte Order in Word.
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word.
47	8001H	2	Maximum number of sectors on Read/Write Multiple command: 1
48	0000H	2	Double Word not supported.
49	0F00H	2	Capabilities: DMA, LBA, IORDY supported
50	4000H	2	Capabilities: device specific standby timer minimum
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	Single Word DMA data transfer cycle timing mode (not supported).
53	0007H	2	Data fields 54-58,64-70 and 88 are valid.
54	XXXX	2	Current numbers of cylinders.
55	XXXX	2	Current numbers of heads.
56	XXXX	2	Current sectors per track.
57-58	XXXX	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW).
59	0100H	2	Multiple sector setting is valid; low byte is capacity dependent.
60-61	XXXX	4	Total number of sectors addressable in LBA Mode.
62	0000H	2	Single Word DMA transfer not implemented
63	0007H	2	Multiword DMA modes 0-2 are supported; upper byte reflects currently selected MWDMA mode.
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum MWDMA cycle time per word is 120ns.
66	0078H	2	Recommended MWDMA cycle time is 120ns.
67	0078H	2	Minimum PIO cycle time without IORDY flow control is 120ns.
68	0078H	2	Minimum PIO cycle time with IORDY flow control is 120ns.
69	8000H	2	CFast specification supported
70-74	0000H	10	Reserved
75	0000H	2	Queue depth of 1 for NCQ
76	0206H	2	Supports Gen 1, Gen2 signaling rates, host initiated power management requests
77	0000H	6	Reserved
78	0008H	2	Device supports initiating interface power management
79	0000H	2	Reserved
80	01FCH	2	Supports ATA5 to ATA8 standard.
81	FFFFH	2	No minor revision reported.
82	742BH	2	Command set: NOP, READ BUFFER, WRITE BUFFER, HPA, volatile write cache, power management feature set, Security Mode feature set, SMART feature set
83	7500H	2	48-bit mode supported; Flush Cache/Flush Cache Ext, LAB48, microcode download supported.
84	4002H	2	World wide name, general purpose logging supported
85	74XXH	2	Feature status
86	B401H	2	Feature status
87	4120H	2	Feature status
88	XX7FH	2	UDMA Modes 0-6 supported.
89	0003H	2	Time for Security Erase Unit
90	0000H	2	Time for Enhanced Security Erase Unit not specified.

Word Address	Default Value	Total Bytes	Data Field Type Information
91	0000H	2	Reserved
92	XXXXH	2	Master password revision code
93-99	0000H	14	Reserved
100-103	XXXXH	8	Maximum user LBA for 48-bit addressing mode.
104-127	0000H	48	Reserved
128	0XXXH	2	Security status
129-159	XXXXH	60	Vendor specific
160	0000H	2	CFA Power mode
161	0000H	2	CFast specific support
162	0000H	2	CPRM not supported
163	0000H	2	CFA Advanced modes: not relevant for CFast
164-216	0000H	2	Reserved
217	0001H	2	Solid State Device
218-255	0000H	8	Reserved

6. S.M.A.R.T. Feature Set

Cactus Technologies® -220 Series Cfast card supports S.M.A.R.T. attribute reporting. This following subcommands are supported when programmed into the Feature Register:

Value	Command	Value	Command
D0h	Read Data	D5h	Reserved
D1h	Read Attribute Threshold	D6h	Reserved
D2h	Enable/Disable Autosave	D8h	Enable SMART operationes
D3h	Save Attribute Values	D9h	Disable SMART operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status

6.1. S.M.A.R.T Data Structure

The Read Data commands returns 512 bytes of data in the following structure:

Byte	Description
0-1	Revision code
2-361	Vendor specific
362	Off-line data collection status
363	Self-test execution status byte
364-365	Total time in seconds to complete off-line data collection activitiies
366	Vendor specific

Byte	Description
367	Off-line data collection capabilities
368-369	SMART capabilities
370	Error logging capabilities: bit[7:1] – reserved; bit[0]: 1=device error logging supported
371	Vendor specific
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374	Convevance self-test routine recommended polling time (in minutes)
375-385	Reserved
386-395	Firmware Version/Date Code
396-397	Reserved
398-399	Reserved
400-406	'SMI2244LT'
407-415	Vendor specific
416	Reserved
417	Program/write the strong page only
418-419	Number of spare block
420-423	Average Erase Count
424-510	Vendor specific
511	Data structure checksum

6.2. S.M.A.R.T Attributes

The following table lists the attributes returned in bytes 2-361 of the 512-byte SMART data:

Attribute ID	Attribute values						Attribute Name
01h	MSB	00	00	00	00	00	Read error rate
05h	LSB	MSB	00	00	00	00	Reallocated sectors count
09h	LSB	MSB	00	00	00	00	Reserved
0Ch	LSB	MSB	00	00	00	00	Power cycle count
A0h	LSB			MSB	00	00	Uncorrectable sector count when read/write
A1h	LSB	MSB	00	00	00	00	Number of valid spare block
A2h	LSB	MSB	00	00	00	00	Number of child pair
A3h	LSB	MSB	00	00	00	00	Number of initial invalid block

Attribute ID	Attribute values						Attribute Name
A4h	LSB			MSB	00	00	Total erase count
A5h	LSB			MSB	00	00	Max. Erase count
A6h	LSB			MSB	00	00	Min. Erase count
A7h	LSB			MSB	00	00	Average erase count
C0h	LSB			MSB	00	00	Power-off retract count
C2h	MSB	00	00	00	00	00	Controlled temperature (fixed at 27C)
C3h	LSB			MSB	00	00	Hardware ECC recovered
C4h	LSB			MSB	00	00	Reallocation event count
C6h	LSB			MSB	00	00	Reserved
C7h	LSB	MSB	00	00	00	00	UltraDMA CRC error count
F1h				MSB	00	00	Total LBAs written (in units of 32MB)
F2h				MSB	00	00	Total LBAs read (in units of 32MB)

Appendix A. Ordering Information

Model KCXF-220S

Where: X is drive capacities:
4G ---------- 4GB
8G ---------- 8GB
16G ---------- 16GB
32G ---------- 32GB
64G ---------- 64GB
128G ---------- 128GB

Example:

(1) 8GB CFast ---------- KC8GF-220S

Appendix B.Technical Support Services

B.1.Direct Cactus Technologies® Technical Support

Cactus Technologies Limited
Suite C, 15/F, Capital Trade Center
62 Tsun Yip Street, Kwun Tong
Kowloon, Hong Kong

Tel: +852-27972261
Fax: +852-27973777
Email: tech@cactus-tech.com

Appendix C.Cactus Technologies® Worldwide Sales Offices

Cactus Technologies Limited
Suite C, 15/F, Capital Trade Center
62 Tsun Yip Street, Kwun Tong
Kowloon, Hong Kong

Tel: +852-27972277
Fax: +852-27973777
Email: sales@cactus-tech.com

US Office:

Cactus USA
3112 Windsor Road , Suite A356
Austin, Texas 78703
Tel: (512) 775 0746
Email: americas@cactus-tech.com

Appendix D.Limited Warranty

I. WARRANTY STATEMENT

Cactus Technologies® warrants its Commercial Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for two years from the date of purchase. This express warranty is extended by Cactus Technologies® Limited to customers of our products.

II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies® responsibilities regarding the Cactus Technologies® Commercial Grade Flash Storage Products. Cactus Technologies®, at its sole option, will repair, replace or refund the purchase price of the defective product. Cactus Technologies® guarantees our products meet all specifications detailed in our product manuals. Although Cactus Technologies® products are designed to withstand harsh environments and have the highest specifications in the industry, they are not warranted to never have failure and Cactus Technologies® does not warranty against incidental or consequential damages. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or backup features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within two years of purchase, Cactus Technologies® will have the option of repairing, replacing or refunding the purchase price the defective product, if the following conditions are met:

A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.

B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty shall be tested to the product’s functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs. Cactus Technologies® Limited may repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

IV. RECEIVING WARRANTY SERVICE

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies® Limited. Please contact Cactus Technologies® Customer Service department (tech@cactus-tech.com) with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies® will issue a Return Material Authorization or Product Repair Authorization number. Ship the defective product to:

Cactus Technologies Limited

Suite C, 15/F, Capital Trade Center

62 Tsun Yip Street, Kwun Tong

Kowloon, Hong Kong