Industrial Grade -910S/910S-P1 series SSD

Product Manual

September 4, 2018

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1.Introduction to Cactus Technologies® Industrial Grade -910S/910S-P1 Series SSD Products

Features:

- Solid state design with no moving parts
- Available in industry standard 2.5” form factor
- Capacities from 64GB to 640GB
- Compliant with Serial ATA 3.0 specifications
- ATA8-ACS2 command set compatible
- Supports Serial ATA Generation I/II/III transfer rate of 1.5/3.0/6.0Gbps
- Supports ATA SMART Feature Set
- Supports ATA Security Feature Set
- Supports SATA NCQ with max. Queue depth of 32
- ECC capable of correcting up to 64 bit errors per 1KB
- Enhanced error correction, < 1 error in 10^{14} bits read
- SATA partial and slumber modes supported
- Voltage support: 5.0V±10%

Enhanced Features for Pro Series (-910S-P1):

- Jumper triggered full disk erase
- AES256 hardware encryption (w/ automatic key erase on power lost, no CryptoErase required)

Cactus Technologies® -910S/910S-P1 series SSD is a high capacity solid-state flash memory product that complies with the Serial ATA 3.0 standard and is functionally compatible with a SATA hard disk drive. Cactus Technologies® -910S/910S-P1 series SSD provide up to 640GB of formatted storage capacity.

Cactus Technologies® -910S/910S-P1 series SSD product uses high quality SLC NAND flash memory from well known vendors, such as Micron Corporation. In addition, it includes an on-drive intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control. The controller’s firmware is upgradeable, thus allowing feature enhancements and firmware updates while keeping the BOM stable.

1.1. Supported Standards

Cactus Technologies® -910S/910S-P1 series SSD is fully compatible with the following specification:

- ATA 8 Specification published by ANSI
- Serial ATA 3.0 Specification published by the Serial ATA International Organization

1.2. Product Features

Cactus Technologies® Industrial SSD contains a high level, intelligent controller. This intelligent controller provides many capabilities including the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

1.2.1. Host and Technology Independence

Cactus Technologies® Industrial SSD appears as a standard SATA disk drive to the host system. The drive utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the drive as per the SATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the drive. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support the Cactus Technologies® Industrial SSD products today will continue to work with future Cactus Technologies® Independence SSDs built with new flash technology without having to update or change host software.

1.2.2. Defect and Error Management

Cactus Technologies® Industrial SSD contains a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies® Industrial SSD is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the drive has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies® Industrial SSDs unparalleled reliability.

1.2.3. Power Supply Requirements

Cactus Technologies® Industrial SSD operates at a voltage range of 5.0 volts ± 10%.

2.Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. Environmental Specifications

		Cactus Technologies® -910S/910S-P1 SSD
Temperature	Operating:	0° C to +70° C (Standard) -45°C to +90°C (extended)
Humidity	Operating & Non-Operating:	8% to 95%, non-condensing
Vibration	Operating & Non-Operating:	20G, MIL-STD-883G Method 2005.2, Condition A
Shock	Operating & Non-Operating:	3,000 G, MIL-STD-883G Method 2002.4, Condition C
Altitude (relative to sea level)	Operating & Non-Operating:	100,000 feet maximum

2.2. System Power Requirements

Table 2-2. Power Requirements

		Cactus Technologies® -910S/910S-P1 SSD
DC Input Voltage (VCC) 100 mV max. ripple (p-p)		5.0V ±10%
(Maximum Average Value) See Notes.	Standby: Reading: Writing:	230 mA 470 mA 660 mA

NOTES: All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all drive inputs are static CMOS levels and in a “Not Busy“ operating state.

2.3. System Performance

All performance timings assume the drive controller is in the default (i.e., fastest) mode.

Table 2-3. Performance

Read Transfer Rate		Up to 430MBytes/sec
Write Transfer Rate	64GB 128GB - 640GB	Up to 225MBytes/sec Up to 440MBytes/sec
IOPS	4K random read (fresh out of box) 4K random read (substained) 4K random write (fresh out of box) 4K random write (substained)	Up to 60K Up to 30K Up to 50K Up to 10K

.

2.4. System Reliability

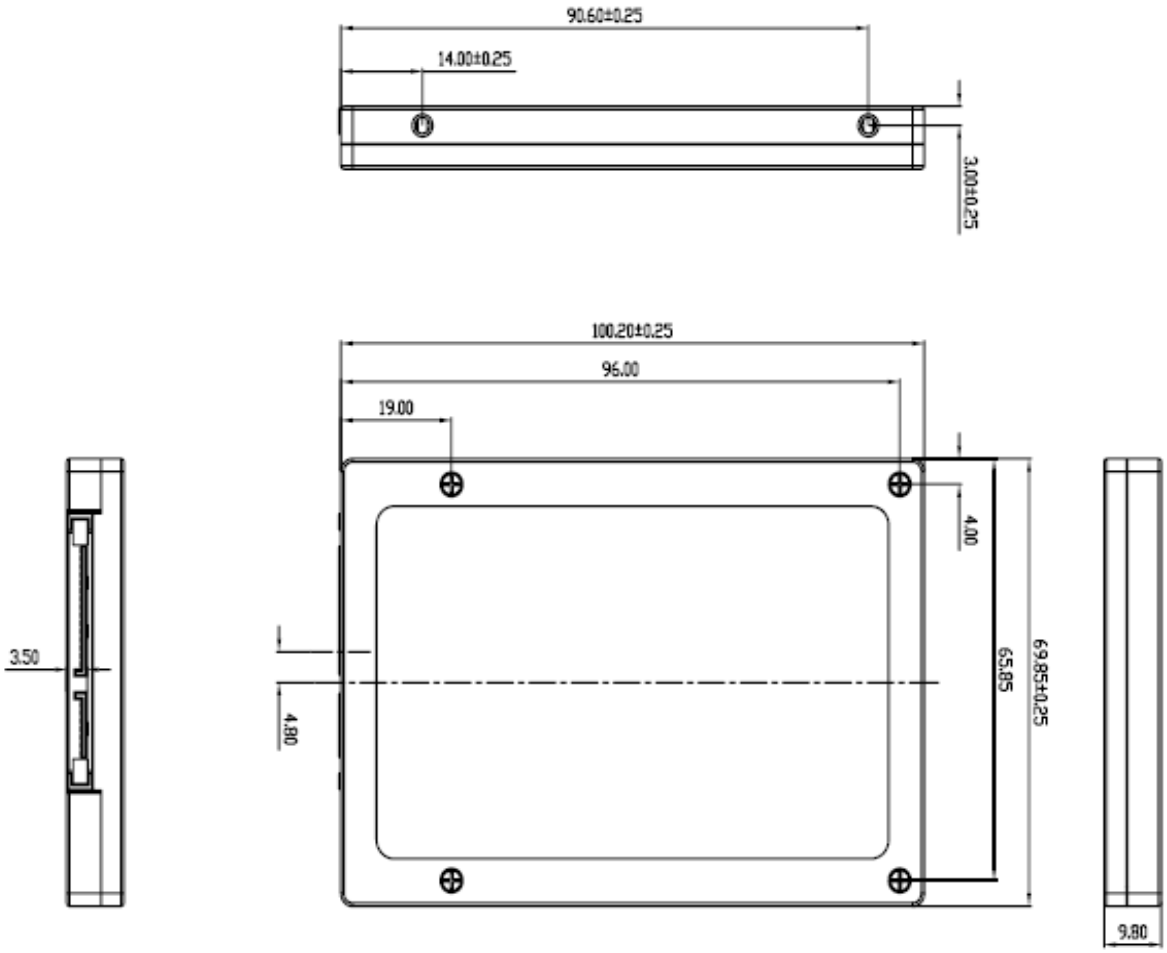
Table 2-4. Reliability

Data Reliability	< 1 non-recoverable error in 10^{14} bits READ
Endurance:	> 2,000,000 erase/program cycles per logical sector

2.5. Physical Specifications

The following sections provide the physical specifications for Cactus Technologies® Industrial SSD products.

2.5.1. 2.5” SSD Physical Specifications



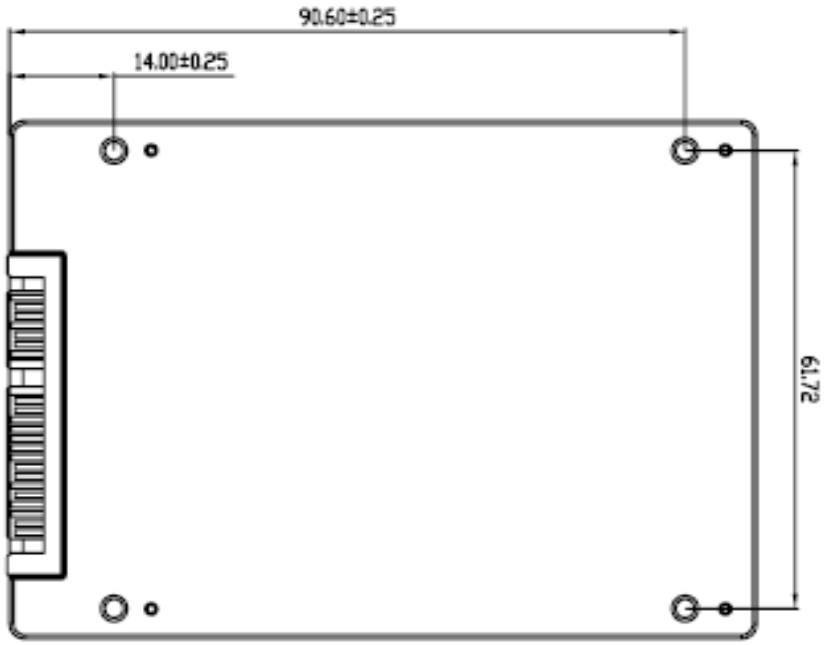


Figure 2-1. 910S 2.5” SSD Dimensions

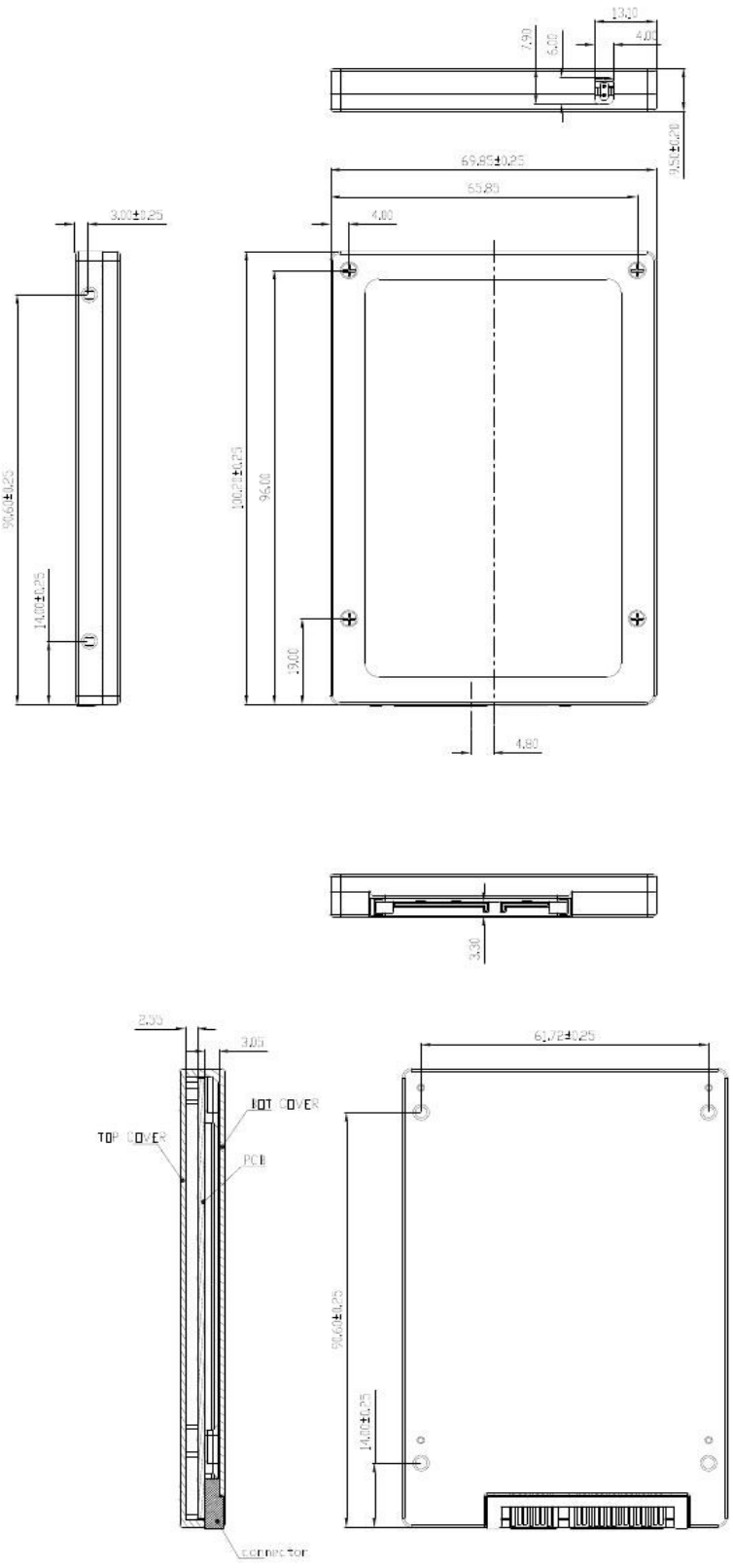


Figure 2-2. 910S-P1 2.5” SSD Dimensions

3.Interface Description

The following sections provide detailed information on the Cactus Technologies® Industrial SSD interface.

3.1. SSD Pin Assignments and Pin Type

Cactus Technologies® SSD uses industry standard 7+12 SATA connector. The signal/pin assignments and descriptions are listed in Table 3-5.

Table 3-5. SSD Pin Assignments and Pin Type

Signal Segment Pin #	Signal Name	Pin Type
S1	GND	
S2	RXP	Analog In
S3	RXN	Analog In
S4	GND	
S5	TXN	Analog Out
S6	TXP	Analog Out
S7	GND	

Power Segment Pin #	Signal Name	Pin Type
P1	3.3V	
P2	3.3V	
P3	3.3V	
P4	GND	
P5	GND	
P6	GND	
P7	5V	
P8	5V	
P9	5V	
P10	GND	
P11	Active LED	
P12	GND	
P13	12V	
P14	12V	
P15	12V	

3.2. Electrical Specifications

The following table defines all D.C. Characteristics for the SSD products. Unless otherwise stated, conditions are:

Vcc = 5.0V ± 10%
Ta = -45°C to 90°C

3.2.1. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Storage Temperature	Ts	-55	+125	°C
Operating Temperature	T_A	-45	+90	°C
Vcc with respect to GND	Vcc	-0.3	5.5	V

3.2.2. DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	Vin	-0.5	Vcc + 0.5	V
Output Voltage	Vout	-0.3	Vcc + 0.3	V
Input Leakage Current	I_{LI}	-10	10	uA
Output Leakage Current	I_{LO}	-10	10	uA
Input/Output Capacitance	C_I/C_o		10	pF
Operating Current	I_{CC}			mA
Sleep Mode			240	
Active			660	

3.2.3. AC Characteristics

Cactus Technologies® Industrial SSD products conforms to all AC timing requirements as specified in the SATA-IO specifications. Please refer to that document for details of AC timing for all operation modes of the device.

4.ATA Drive Register Set Definition and Protocol

The communication to or from the SSD is done using FIS. Legacy ATA protocol is supported by using the legacy mode defined in the SATA specifications. In this mode, the FIS has defined fields which provide all the necessary ATA task file registers for control and status information. The Serial ATA interface does not support Primary/Secondary or Master/Slave configurations. Each SATA channel supports only one SATA device, with the register selection as defined by the ATA standard.

4.1. ATA Task File Definitions

The following sections describes the usage of the ATA task file registers. Note that the Alternate Status Register of legacy ATA is not defined for SATA drives.

4.1.1. Data Register

The Data Register is a 16-bit register, and it is used to transfer data blocks between the SSD data buffer and the Host.

4.1.2. Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

4.1.3. Feature Register

This register provides information regarding features of the SSD that the host can utilize.

4.1.4. Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the SSD. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

4.1.5. Sector Number (LBA 7-0) Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any SSD data access for the subsequent command.

4.1.6. Cylinder Low (LBA 15-8) Register

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

4.1.7. Cylinder High (LBA 23-16) Register

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

4.1.8. Drive/Head (LBA 27-24) Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.
Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.
Bit 5 This bit is set to 1.
Bit 4 (DRV) DRV is the drive number. This should always be set to 0.
Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

4.1.9. Status Registers

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the device has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.
Bit 6 (RDY) RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the device is ready to accept a command.
Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.
Bit 4 (DSC) This bit is set when the device is ready.
Bit 3 (DRQ) The Data Request is set when the device requires that information be transferred either to or from the host through the Data register.
Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
Bit 1 (IDX) This bit is always set to 0.
Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

4.1.10. Device Control Register

This register is used to control the drive interrupt request and to issue an ATA soft reset to the drive. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
HOB	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is used in 48-bit addressing mode. When cleared, the host can read the most recently written values of the Sector Count,Drive/Head and LBA registers. When set, the host will read the previous written values of these registers. A write to any Command block register will clear this bit.

Bit 6 This bit is an X (Do not care).

Bit 5 This bit is an X (Do not care).

Bit 4 This bit is an X (Do not care).

Bit 3 This bit is ignored by the drive.

Bit 2 (SW Rst) This bit is set to 1 in order to force the drive to perform an AT Disk controller Soft Reset operation. The drive remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the drive are disabled. This bit is set to 0 at power on and Reset.

Bit 0 This bit is ignored by the drive.

4.1.11. Drive Address Register

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.

Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the SSD. Following are some possible solutions to this problem:

1. Locate the SSD at a non-conflicting address (i.e., Secondary address (377) when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and a SSD in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a SSD product is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the SSD's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the SSD or b) if provided use an additional Primary/Secondary configuration in the SSD that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.

Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.

Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

5.ATA Command Description

This section defines the ATA command set supported by Cactus Technologies® -910S/910S-P1 series SSDs.

5.1. ATA Command Set

Table 5-6 summarizes the supported ATA command set .

Table 5-6. ATA Command Set

COMMAND	Code
Check Power Mode	E5h, 98h
Device Reset	08h
Device Configuration	-
Device Configuration Freeze Lock	B1h/C1h
Device Configuration Identify	B1h/C2h
Device Configuration Restore	B1h/C0h
Device Configuration Set	B1h/C3h
Download Microcode	92h
Data Set Management	06h
Execute Drive Diagnostic	90h
Flush Cache	E7h
Flush Cache Ext	EAh
Identify Drive	ECh
Idle	E3h, 97h
Idle Immediate	E1h, 95h
Initialize Drive Parameters	91h
NOP	00h
Read Buffer	E4h
Read DMA	C8h
Read DMA Ext	25h
Read FDPMA Queued	60h
Read Log Ext	2Fh
Read Multiple	C4h
Read Multiple Ext	29h
Read Native Max Address	F8h
Read Native Max Address Ext	27h
Read Sector(s)	20h
Read Sector(s) Ext	24h
Read Verify Sector(s)	40h
Read Verify Sector(s) Ext	42h
Security Disable Password	F6h
Security Erase Prepare	F3h
Security Erase Unit	F4h
Security Freeze Lock	F5h
Security Set Password	F1h
Security Unlock	F2h
Seek	70h
Set Features *	EFh

COMMAND	Code
Set Transfer Mode	EFh/03h
Enable Power-up In Standby	EFh/06h
Disable Power-up In Standby	EFh/08h
Set Max	
Set Max Address	F9h
Set Max Freeze Lock	F9h/04h
Set Max Lock	F9h/02h
Set Max Set Password	F9h/01h
Set Max Unlock	F9h/03h
Set Max Address Ext	37h
Set Multiple Mode	C6h
Set Sleep Mode	E6h, 99h
SMART	
SMART Disable Operations	B0h/D9h
SMART Enable Operations	B0h/D8h
SMART Enable/Disable Attribute Autosave	B0h/D2h
SMART Execute Off-line Immediate	B0h/D4h
SMART Read Attribute Thresholds	B0h/D1h
SMART Read Data	B0h/D0h
SMART Read Log	B0h/D5h
SMART Return Status	B0h/DAh
SMART Save Attribute Values	B0h/D3h
SMART Write Log	B0h/D6h
Stand By	E2h, 96h
Stand By Immediate	E0h, 94h
Soft Reset	FFh
Write Buffer	E8h
Write DMA	CAh
Write DMA Ext	35h
Write FPDMA Queued	61h
Write Log Ext	3Fh
Write Multiple	C5h
Write Multiple Ext	39h
Write Sector(s)	30h
Write Sector(s) Ext	34h
Vendor Specific CMD	FEh

**** Note that 910S/910S-P1 series SSDs write cache is always enabled. Enable/Disable Cache through the Set Features command has no effect on write caching.***

5.1.1. Identify Drive—ECH

The Identify Drive command enables the host to receive parameter information from the drive. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 5-7. All reserved bits or words are zero. Table 5-7 is the definition for each field in the Identify Drive Information.

Table 5-7. Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	0040H	2	Non-removable device.
1	XXXXH	2	Default number of cylinders; capacity dependent.
2	XXXXH	2	Reserved
3	00XXH	2	Default number of heads; capacity dependent.
4-5	0000H	4	Retired
6	XXXXH	2	Default number of sectors per track; capacity dependent.
7-8	XXXXH,XXXXH	4	Reserved
9	0000H	2	Retired
10-19	aaaa	20	Serial number in ASCII (Right Justified).
20	0000H	2	Retired
21	0000H	2	Retired
22	0000H	2	Obsolete
23-26	aaaa	8	Firmware revision in ASCII . Big Endian Byte Order in Word.
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word.
47	8001H	2	Maximum number of sectors on Read/Write Multiple command: 1
48	0000H	2	Reserved
49	2F00H	2	Capabilities: DMA, LBA, IORDY supported
50	4000H	2	Capabilities: device specific standby timer minimum
51	0000H	2	PIO data transfer cycle timing mode
52	0000H	2	Single Word DMA data transfer cycle timing mode (not supported).
53	0007H	2	Field validity.
54	XXXX	2	Current numbers of cylinders.
55	XXXX	2	Current numbers of heads.
56	XXXX	2	Current sectors per track.
57-58	XXXX	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW).
59	0101H	2	Multiple sector setting is valid; multiple count is 1.
60-61	XXXX	4	Total number of sectors addressable in LBA Mode.
62	0000H	2	Obsolete
63	0007H	2	Multiword DMA modes 0-2 are supported; upper byte reflects currently selected MWDMA mode.
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum MWDMA cycle time per word is 120ns.
66	0078H	2	Recommended MWDMA cycle time is 120ns.
67	0078H	2	Minimum PIO cycle time without IORDY flow control is 120ns.
68	0078H	2	Minimum PIO cycle time with IORDY flow control is 120ns.
69	4000H	2	Deterministic data after TRIM supported.
70-74	XXXXH	10	Reserved
75	001FH	2	Queue depth of 32 for NCQ
76	050EH	2	SATA capabilities – PHY Event Counters, NCQ supported; SATA Gen1,2,3 signaling speeds supported
77	000XH	2	Lower byte reflects current SATA signal speed
78	0044H	2	Support of SerialATA functions
79	00XXH	2	Serial ATA functions enabled
80	001EH	2	Major revision number – ATA8-ACS; ATA 7,6,5 supported
81	0000H	2	Minor revision number
82	346BH	2	Command set supported
83	7D01H	2	Command set supported
84	4122H	2	Command set/feature supported extension
85	3469H	2	Command set/feature enabled (values may differ depending on features enabled).
86	3C01H	2	Command set/feature enabled (values may differ depending on features enabled).
87	4122H	2	Command set/feature enabled (values may differ depending on features enabled).

Word Address	Default Value	Total Bytes	Data Field Type Information
88	407FH	2	UDMA Modes 0-6 supported; upper byte reflects currently selected mode.
89	0001H	2	Security Erase Unit time.
90	0001H	2	Enhanced Security Erase Unit time.
91	0000H	2	Current APM level.
92	FFFEH	2	Master password revision code
93	0000H	2	Hardware reset default
94-99	0000H	12	Reserved
100-103	XXXXH	8	Maximum user LBA for 48-bit addressing mode.
104	0000H	2	Reserved
105	0001H	2	Max. block of LBA Range Entries per TRIM command.
106	4000H	2	Physical sector size per sector
107-116	0000H	20	Reserved
117-118	0100H	4	# of words for logical sectors
119	0000H	2	Features supported.
120	0000H	2	Features supported or enabled.
121-127	0000H	12	Reserved
128	00XXH	2	Security status.
129-159	0000H	60	Vendor specific.
160-167	0000H	16	Reserved for CFA.
168	0000H	2	Form factor.
169	0001H	2	TRIM supported.
170-205	0000H	72	Reserved
206	0000H	2	SCT command set not supported.
207-216	0000H	20	Reserved
217	0001H	2	Reserved
218-221	0000H	8	Reserved
222	103FH	2	Transport mode version number
223-254	0000H	44	Reserved
255	XXXXH	2	Checksum

6. S.M.A.R.T. Feature Set

Cactus Technologies® -910/910S-P1 Series SSDs supports S.M.A.R.T. attribute reporting. This following subcommands are supported when programmed into the Feature Register:

Value	Command	Value	Command
D0h	Read Data	D6h	SMART Write Log
D2h	Enable/Disable Autosave	D8h	Enable SMART operations
D3h	Save Attribute Values	D9h	Disable SMART operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status
D5h	SMART Read Log		

6.1. S.M.A.R.T Data Structure

The Read Data commands returns 512 bytes of data in the following structure:

Byte(s)	Description
0-1	Revision code
2-361	Data for attributes 1 - 30
362	Off-line data collection status
363	Self-test execution status byte
364-365	Total time in seconds to complete off-line data collection activities
366	Vendor specific
367	Off-line data collection capabilities
368-369	SMART capabilities
370	Error logging capabilities: bit[7:1] – reserved: bit[0]: 1=device error logging supported
371	Vendor specific
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374-510	Reserved
511	Data structure checksum

6.2. S.M.A.R.T Attribute Data Structure

Each attribute returned in bytes 2-361 of the 512-byte SMART data has the following format:

Byte(s)	Descriptions
0	Attribute ID
1 – 2	Flags
3 – 10	Attribue value
11	Reserved

6.3. S.M.A.R.T Attributes

The S.M.A.R.T attributes returned by the Read Data command are listed below:

Attribute ID	Attribute Name	Description
01h	Raw Read error rate	Read retry count
09h	Power-on hours	Total time of power-on state in hours
0Ch	Power cycle count	Number of power on/off cycles

Attribute ID	Attribute Name	Description
0Dh	Soft Read error rate	Corrected ECC error events which exceeded warning ECC error threshold
AFh	Program Failure Block Count	Number of flash program failures
B0h	Erase Failure Block Count	Number of flash erase failures
B8h	Initial bad block count	Number of initial bad blocks detected during fimrware install
B9h	Current bad block count	Number of current bad blocks
C0h	Unexpected Power Shutdown Count	Number of unexpected power outages when the device was shutdown without prior “STANDBY IMMEDIATE” command
C2h	Temperature	Current device temperature in □C
C7h	Read Failure count	Number of uncorrectable read failures
C8h	Total Write count	Total number of write commands issued
C9h	Total Read count	Total number of read commands issued
CAh	Total write sector count requested by host	Total number of sectors written as requested by the host
CBh	Total write sector count as written to flash	Total number of sectors written to flash
CCh	Total read sector count requested by host	Total number of sectors read from the host
D1h	SSD life remaining	Approximate SSD life left (Max. PE cycle – avg. Erase count) / Max. PE cycle
D2h	Min. erase count	Lowest erase count of all flash blocks
D3h	Max. erase count	Highest erase count of all flash blocks
D4h	Avg. erase count	Average erase count of all flash blocks
D5h	Max. PE count	Maximum allowed Program/Erase count
DDh	Bad block full	Returns '1' when total bad block count exceeds 5% of all banks
DFh	SATA CRC error count	Number of SATA interface CRC errors
E0h	SATA handshake error count	Number of SATA interface handshake errors

6.4. S.M.A.R.T Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature.

6.5. S.M.A.R.T Execute Off-line Immediate (subcommand D4h)

This subcommand causes the device to start the off-line process for the requested mode and operation. The LBA Low register shall be set to specify the operation to be executed as follows:

LBA Low value	Description
00h	Execute SMART off-line data collection routine immediately
01h	Execute SMART short self-test routine immediately in off-line mode
02h	Execute SMART Extended self-test routine immediately in off-line mode
03h	Reserved
04h	Execute SMART Selective self-test routine immediately in off-line mode
40h	Reserved
7Fh	Abort off-line mode self-test routine
81h	Execute SMART short self-test routine immediately in captive mode
82h	Execute SMART Extended self-test routine immediately in captive mode
84h	Execute SMART Selective self-test routine immediately in captive mode
C0h	Reserved

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte and ATA registers and then executes the command completion. Taskfile registers will have return values as follows:

STATUS reg: Set ERR to one when self-test failed

ERR reg: Set ABRT to one when self-test failed

LBA LOW reg: Set to F4h when self-test failed

LBA HIGH reg: Set to 2Ch when self-test failed

6.6. S.M.A.R.T Read Log (subcommand D5h)

This command returns the specified log sector content to the host. LBA Low and Sector Count registers shall be set to specify the log sector and sector number to be written.

LBA Low value	Sector Count	Content	
00h	1	Log directory	Read only
01h	1	SMART error log	Read only
02h	1	Comprehensive SMART error log	Read only
04h-05h	-	Reserved	Read only
06h	1	SMART self-test log	Read only
08h	-	Reserved	Read only
09h	1	Selective self-test log	R/W
0Ah-7Fh	-	Reserved	Read only
80h-9Fh	16	Host vendor specific	R/W
A0h-Ffh	-	Reserved	Vendor specific

6.6.1. S.M.A.R.T Log Directory Structure

Byte(s)	Description
0-1	SMART log version (set to 01h)
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved
6-509	Number of sector in the log at log addresses 2 to 254
510	Number of sectors in the log at log address 255
511	Reserved

6.6.2. S.M.A.R.T Error Log Structure

Byte(s)	Description
0	SMART error log version (set to 01h)
1	Error log index
2-91	1st error log data structure
92-181	2nd error log data structure
182-271	3rd error log data structure
272-361	4th error log data structure
362-451	5th error log data structure
452-453	Device error count
454-510	Reserved
511	Checksum

Error log data structure (where n is 1 to 5):

Byte(s)	Description
n - n+11	1st command data structure
n+12 – n+23	2nd command data structure
n+24 – n+35	3rd command data structure
n+36 – n+47	4th command data structure
n+48 – n+59	5th ommand data structure
n+60 – n+89	Error data structure

Command data structure:

Byte	Description
0	Content of Device Control register when the Command register was written
1	Content of Feature Control register when the Command register was written
2	Content of Sector Count register when the Command register was written
3	Content of LBA Low register when the Command register was written
4	Content of LBA Mid register when the Command register was written
5	Content of LBA High register when the Command register was written

6	Content of Device/Head register when the Command register was written
7	Content written to Command register
8	Timestamp
9	Timestamp
10	Timestamp
11	Timestamp

Error data structure:

Byte	Description
0	Reserved
1	Content of Error register after command completion
2	Content of Sector Count register after command completion
3	Content of LBA Low register after command completion
4	Content of LBA Mid register after command completion
5	Content of LBA High register after command completion
6	Content of Device/Head register after command completion
7	Content of Status register after command completion
8-26	Extended error information
27	State
28	Timestamp (LSB)
29	Timestamp (MSB)

State values:

Value	State
X0h	Unknown
X1h	Sleep
X2h	Standby
X3h	Active or IDLE with BSY cleared
X4h	Executing SMART off-line or self-test
X5h-XAh	Reserved
Xbh-Xfh	Vendor specific

6.6.3. Self-test Log Structure

Byte(s)	Description
0-1	Log version
2+n*24	Self-test number
3+n*24	Self-test status
4+n*24 - 5+n*24	timestamp
6+n*24	Self-test failure checkpoint
7+n*24 - 10+n*24	LBA of first failure
11+n*24 - 25+n*24	Vendor specific
----	----
506-507	Vendor specific
508	Self-test log pointer
509-510	Reserved
511	Checksum

n is 0 through 20.

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

7.Additional Features for -910S-P1

Cactus Technologies® -910S-P1 series SSDs support the following additional features:

- jumper triggered full disk erase
- AES256 hardware encryption

7.1. Jumper Triggered Full Disk Erase

A hardware jumper is located at the back of the drive chassis. When the two pins are shorted together for a duration of 60ms or more, it will trigger an internal full disk erase operation. This erase operation will erase all user accessible blocks and any re-assigned/spare blocks that may have contained user data. The drive's firmware is not erased and the drive will remain usable after the erase operation.

Once the erase operation has started, it cannot be interrupted. If the device is powered off while a quick erase operation is in progress, upon the next power up, the drive will resume the erase operation from where it left off when power was lost.

The erase procedure used by default is DoD-5220. The time it takes to complete varies by drive capacity but will generally between 20-30mins.

An optional quick erase procedure is supported, which will typically take around 30-60s to complete. Customers who wish to use this erase procedure instead of the default DoD-5220 should contact the factory for details.

7.2. AES256 Hardware Encyrption

Cactus Technologies® -910S-P1 series SSDs support hardware AES256 encryption/decryption. A unique feature of the implementation of encryption in the -910S-P1 series SSDs is that the encryption key is not saved in non-volatile storage on the drive, thus there is no possibility of the key being retrieved/hacked by 3rd party if the drive is stolen.

The features of the hardware encryption are as follows:

- host sends over encryption key to the drive via a Vendor Specific command
- the drive will generate a hash sum from the key and store this hash sum to reserved area in the drive;
- The encryption key is stored only in volatile DRAM and will be erased once the drive is powered off
- once the key has been accepted by the device, host will power cycle the drive which will enable the encryption and drive locking features
- once encryption is enabled, host must resend encryption key on power up; a hash sum is generated from the key and verified against the hash sum stored in the reserved area; decryption function is enabled only if the hash sums matches
- if incorrect key is entered three times in a row, an automatic secure erase will be triggered and all user data on the drive will be erased
- once encryption is enabled, the only way to disable it is via a ATA Security Erase operation, which will result in all user data being erased also

7.2.1. Vendor Specific Command

To enable encryption function, host needs to issue the following Vendor Specific command to the drive:

	7	6	5	4	3	2	1	0
Features	N/A							

	7	6	5	4	3	2	1	0
Sector Count	N/A							
LBA Low	N/A							
LBA Med	N/A							
LBA High	N/A							
Device/Head	N/A			Dev	N/A			
Command	FEh							

Host must then perform a single sector PIO Data Out operation to the drive. The format of the sector data is as follows:

Word	Description
0-15	AES key (32 bytes)
16-255	reserved

After the drive has received this data, it will return status information via the task file registers as follows:

	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
LBA Low	N/A							
LBA Med	Command Status							
LBA High	N/A							
Device/Head	N/A			Dev	N/A			
Status	BSY	DRDY	DF	N/A	DRQ	N/A		ERR

The values returned for Command Status are as follows:

0 – Success
1 – Incorrect key
2 – key command aborted (due to same key issued after correct key already accepted)

7.2.2. Enabling and Using Encryption

Here are the recommended steps to enable and use the AES256 hardware encryption feature:

1. Start with a blank drive – any data that existed before encryption is enabled will be lost once encryption is enabled as the data will be scrambled when sent through the decryption engine.

2. Setup encryption key and power cycle the drive – the drive is now encryption enabled and locked

3. Enter correct key – this will unlock the drive, it will appear to the host as a raw, unpartitioned drive

4. Create a new partition and format the drive

5. The drive is now ready for use.

6. Upon power cycle, the encryption key must be re-sent and the drive will be usable again.

How the host system behaves after the correct encryption key is sent to the drive varies from system to system, depending on the combination of BIOS, Chipset, OS and device driver. On some systems, the drive will be automatically detected and mounted while in others, it may be necessary to do a manual re-scan of the disks. Below are examples of how to do manual disk re-scan for Windows and Linux:

- Windows

  Open Disk Management Tool. Sometimes this will automatically cause the drive to be detected and mounted. If this does not happen, click on an empty spot in the Disk Management window, then select 'Action' menu and click 'Refresh'; the drive will be detected and mounted. Alternately, one can also use the 'rescan' option of Diskpart command line tool.

- Linux

  In Linux, the system will detect the drive as a raw disk. It is necessary to delete the entry of this disk from the OS and do a re-scan. The following steps are for Fedora.

  As root, issue the following command:

  ```
  echo 1 > /sys/block/<dev>/device delete
  ```

  where <dev> is the device name (e.g. sda, sdb, etc.)

  Next, find out the host# where the drive is attached; this can be done by issuing the following command:

  ```
  readlink /sys/block/<dev>
  ```

  Where <dev> is the same device name used in the 1st command. Next, issue the following command as root:

```
echo “- - -” > /sys/class/scsi_host/host<n>/scan
```

Where `host<n>` is that host channel where the drive is attached to (e.g. host0, host 1, etc.). This will force the OS to rescan for any disk attached to that host channel. The drive will then be detected and automatically mounted.

Appendix A. Ordering Information

Model KDXFY-910S-P1

Where: X is drive capacities:

64G ---------- 64GB
128G ---------- 128GB
160G ---------- 160GB
256G ---------- 256GB
320G ---------- 320GB
512G ---------- 512GB
640G ---------- 640GB

Where Y is temperature grade:

blank ---------- standard (0℃ to 70℃)
I ---------- extended (-45℃ to 90℃)

Where P1 is drive option:

blank ---------- standard version
P1 ---------- Pro version

Example:

(1) 128GB 2.5” SSD ---------- KD128GF-910S
(2) 128GB extended temp. SSD ---------- KD129GFI-910S
(3) 256GB 2.5” SSD Pro Series ---------- KD256GF-910S-P1

Appendix B.Technical Support Services

B.1.Direct Cactus Technologies® Technical Support

Email: tech@cactus-tech.com

Appendix C.Cactus Technologies® Worldwide Sales Offices

Email: sales@cactus-tech.com

Email: americas@cactus-tech.com

Appendix D.Limited Warranty

I. WARRANTY STATEMENT

Cactus Technologies® warrants its Industrial Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for five years from the date of purchase. This express warranty is extended by Cactus Technologies® Limited to customers of our products.

II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies® responsibilities regarding the Cactus Technologies® Industrial Grade Flash Storage Products. Cactus Technologies®, at its sole option, will repair, replace or refund the purchase price of the defective product. Cactus Technologies® guarantees our products meet all specifications detailed in our product manuals. Although Cactus Technologies® products are designed to withstand harsh environments and have the highest specifications in the industry, they are not warranted to never have failure and Cactus Technologies® does not warranty against incidental or consequential damages. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or backup features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within five years of purchase, Cactus Technologies® will have the option of repairing, replacing or refunding the purchase price the defective product, if the following conditions are met:

A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.

B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty shall be tested to the product’s functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs. Cactus Technologies® Limited may repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

IV. RECEIVING WARRANTY SERVICE

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies® Limited. Please contact Cactus Technologies® Customer Service department (tech@cactus-tech.com) with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies® will issue a Return Material Authorization or Product Repair Authorization number with return shipping instructions.