Industrial Grade
-900S series
mSATA SSD

Product Manual

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1.Introduction to Cactus Technologies® Industrial Grade -900S Series mSATA SSD Products

Features:

- Solid state design with no moving parts
- Industry standard mSATA form factor
- Capacities from 4GB to 128GB
- Compliant with Serial ATA 2.6 specifications
- ATA-8 compatible
- Supports Serial ATA Generation I/II transfer rate of 1.5/3.0Gbps
- Support ATA SMART Feature Set
- Support ATA Security Feature Set
- ECC capable of correcting up to 8 random bit errors per sector or 24 random bit errors per 1KB
- High reliability, MTBF > 4,000,000 hrs.
- Enhanced error correction, < 1 error in 10^{14} bits read
- SATA partial and slumber modes supported
- Voltage support: 3.3V±5%
- Optional 'lidded' version for enhanced protection against the environment

Cactus Technologies® mSATA SSD is a high capacity solid-state flash memory product that complies with the Serial ATA 2.6 standard and is functionally compatible with a SATA hard disk drive. Cactus Technologies® mSATA SSDs provide up to 128GB of formatted storage capacity.

Cactus Technologies® mSATA product uses high quality SLC NAND flash memory from well known vendors, such as Toshiba Corporation. In addition, it includes an on-drive intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control. The controller's firmware is upgradeable, thus allowing feature enhancements and firmware updates while keeping the BOM stable.

1.1. Supported Standards

Cactus Technologies® mSATA SSD is fully compatible with the following specification:

- ATA 8 Specification published by ANSI
- Serial ATA 2.6 Specification published by the Serial ATA International Organization

1.2. Product Features

Cactus Technologies® Industrial mSATA SSD contains a high level, intelligent controller. This intelligent controller provides many capabilities including the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

1.2.1. Host and Technology Independence

Cactus Technologies® Industrial mSATA SSD appears as a standard SATA disk drive to the host system. The drive utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the drive as per the SATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the drive. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support Cactus Technologies® Industrial mSATA products today will continue to work with future Cactus Technologies® Industrial mSATA products built with new flash technology without having to update or change host software.

1.2.2. Defect and Error Management

Cactus Technologies® Industrial mSATA SSD contains a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies® Industrial mSATA SSD is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the drive has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies® Industrial mSATA SSDs unparalleled reliability.

1.2.3. Power Supply Requirements

Cactus Technologies® Industrial mSATA SSD operates at a voltage range of 3.3 volts ± 5%.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. Environmental Specifications

		Cactus Technologies® Industrial mSATA
Temperature	Operating:	0° C to +70° C (Standard) -45° C to +90° C (Extended)
Humidity	Operating & Non-Operating:	8% to 95%, non-condensing
Vibration	Operating & Non-Operating:	20G, MIL-STD-883G Method 2005.2, Condition A
Shock	Operating & Non-Operating:	3,000 G, MIL-STD-883G Method 2002.4, Condition C
Altitude (relative to sea level)	Operating & Non-Operating:	100,000 feet maximum

2.2. System Power Requirements

Table 2-2. Power Requirements

		Cactus Technologies® Industrial mSATA
DC Input Voltage (VCC) **100 mV max. ripple (p-p)**		3.3V ±5%
(Maximum Average Value) **See Notes.**	Sleep: Reading: Writing:	80 mA 240 mA 260 mA

NOTES: All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all drive inputs are static CMOS levels and in a “Not Busy“ operating state.

2.3. System Performance

All performance timings assume the drive controller is in the default (i.e., fastest) mode.

Table 2-3. Performance

Read Transfer Rate		Up to 100MBytes/sec
Write Transfer Rate		Up to 90 Mbytes/sec

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2.4. System Reliability

Table 2-4. Reliability

MTBF (@ 25°C)	> 4,000,000 hours
Data Reliability	< 1 non-recoverable error in 10^{14} bits READ
Endurance:	> 2,000,000 erase/program cycles per logical block

2.5. Physical Specifications

The following sections provide the physical specifications for Cactus Technologies® Industrial mSATA products.

2.5.1. mSATA SSD Physical Specifications

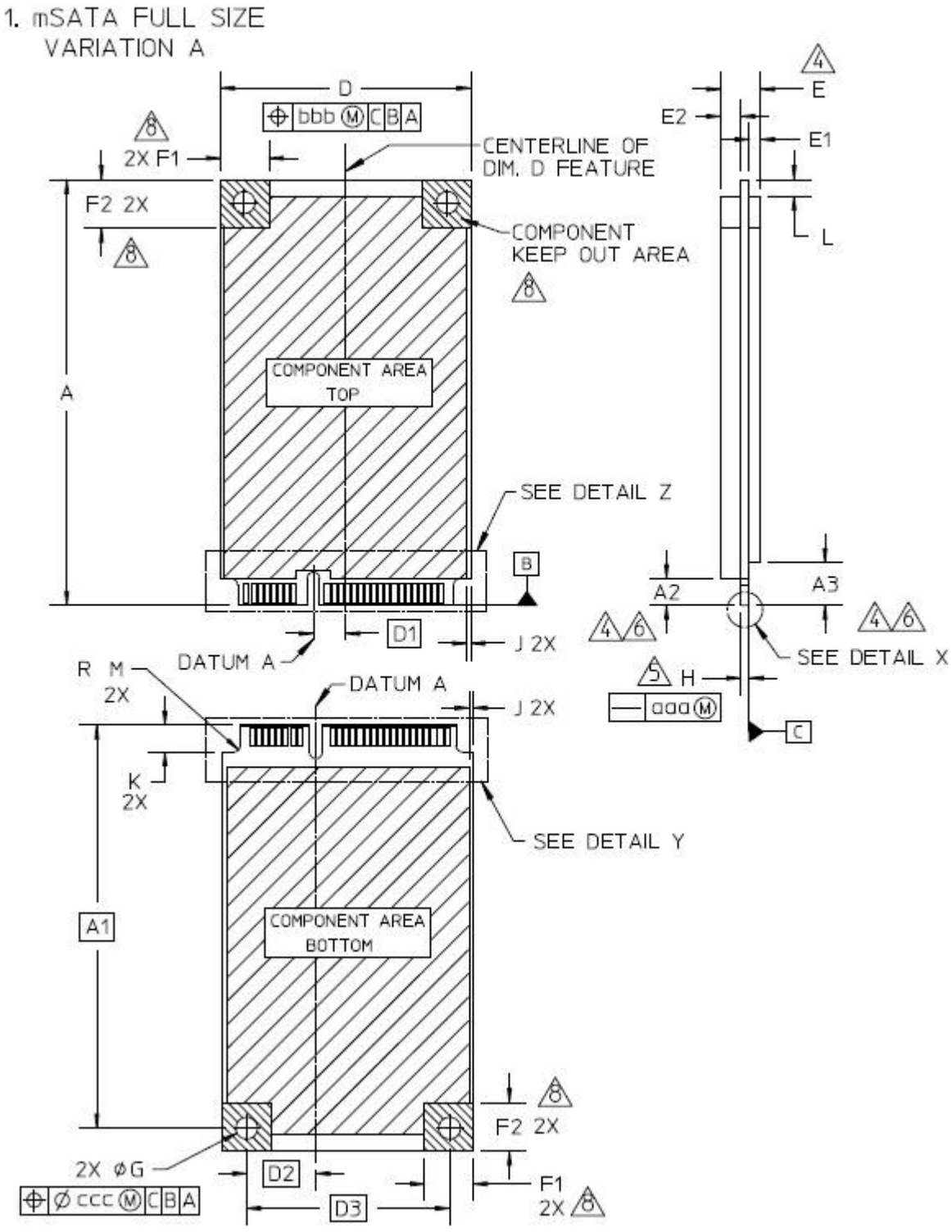
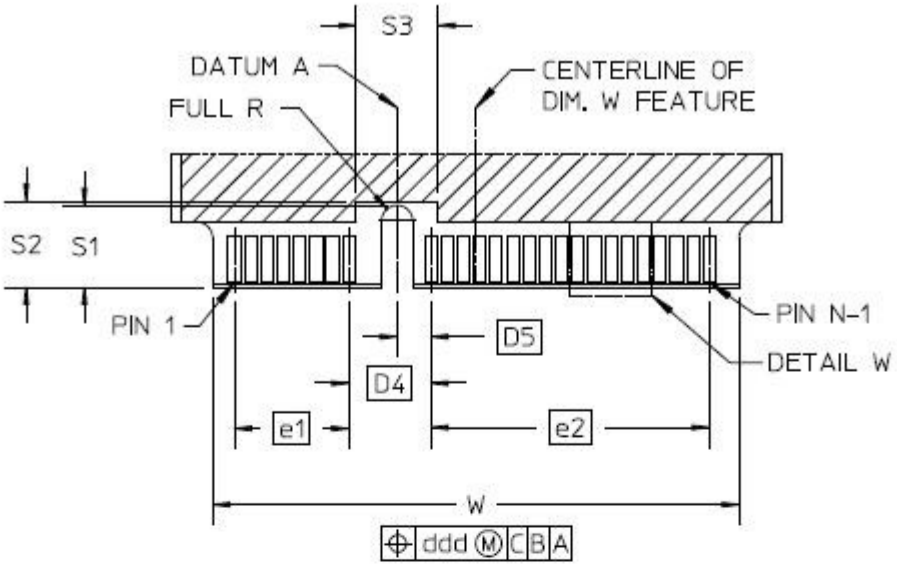
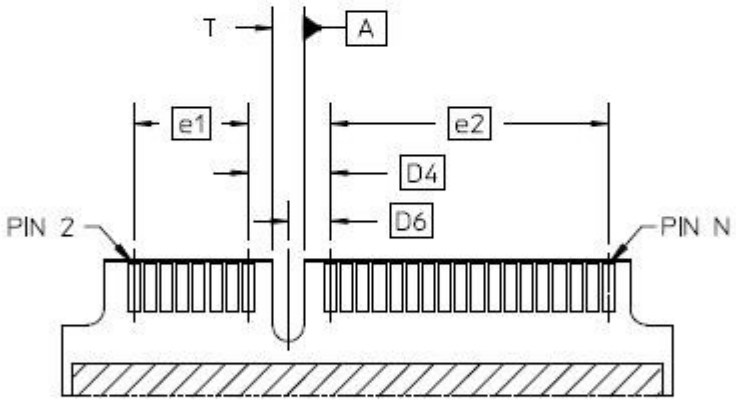


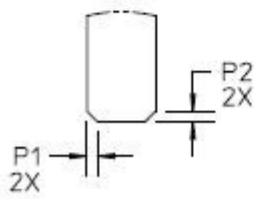
Figure 2-1. mSATA SSD Dimensions



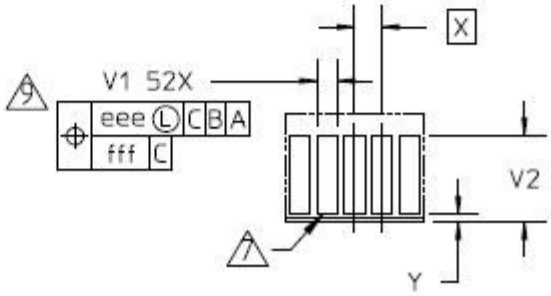
DETAIL Z



DETAIL Y



DETAIL X



DETAIL W

TABLE 1

COMMON DIMENSION TABLE				
SYMBOL	MIN	NOM	MAX	NOTES
A2	3.20	–	–	4,6
A3	5.10	–	–	4,6
D	29.70	29.85	30.00	
G	2.50	2.60	2.70	
H	0.90	1.00	1.10	5
J	0.50	–	–	
K	3.20	–	–	
M	–	–	0.80	
P1	–	–	0.25	
P2	–	–	0.25	
S1	3.90	4.00	4.10	
S2	4.20	–	–	
S3	4.00	–	–	
T	1.40	1.50	1.60	
V1	0.55	0.60	0.65	
V2	2.40	2.55	2.70	
W	25.55	25.70	25.85	
Y	–	–	0.25	
N		52		
ISSUE	A			
REF	14-131			
NOTES	1, 2, 3			

TABLE 2

GD&T BASIC DIMENSIONS		
SYMBOL	VALUE	NOTES
D1	3.85	
D2	8.25	
D3	24.20	
D4	4.00	
D5	1.65	
D6	2.05	
e1	5.60	
e2	13.60	
X	0.80	
ISSUE	A	
REF	14-131	
NOTES	1, 2, 3	

TABLE 3

TOLERANCES OF FORM AND POSITION		
SYMBOL	VALUE	NOTES
aaa	0.22	
bbb	0.10	
ccc	0.10	
ddd	0.10	
eee	0.10	
fff	0.05	
ISSUE	A	
REF	14-131	
NOTES	1, 2, 3	

TABLE 4

	mSATA FULL SIZE VARIATION A		
SYMBOL	MIN	NOM	MAX
A	50.65	50.80	50.95
A1	48.05 BASIC		
E	–	–	4.85
E1	–	–	1.35
E2	–	–	2.40
F	–	–	–
F1	5.65	5.80	5.95
F2	5.65	5.80	5.95
L	2.00	–	–
ISSUE	A		
REF	14-131		
NOTES	1, 2, 3		

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

2. TOLERANCES ON ALL DIMENSIONS ±0.15 UNLESS OTHERWISE SPECIFIED.

3. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.

4. DIMENSIONS APPLICABLE WHEN COMPONENTS ARE MOUNTED ON BOTH SIDES.

5. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

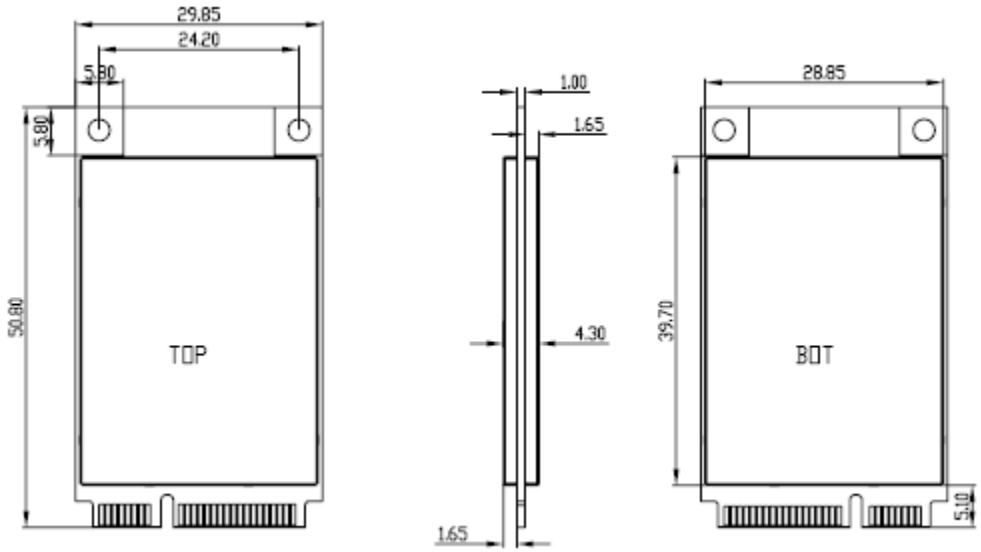
6. BORDER OF COMPONENT AREA.

7. EDGE OF CONTACT PADS SHALL BE FREE OF BURRS AND EXTERNAL TIE BARS.

8. COMPONENT AND ROUTING (TOP/BOTTOM LAYER) KEEP OUT AREA FOR HOLD DOWN SOLUTIONS.

2.5.2. mSATA SSD lidded version Physical Specifications

The following is mechanical dimensions of the 'lidded' version mSATA:



3. Interface Description

The following sections provide detailed information on Cactus Technologies® Industrial mSATA SSD interface.

3.1. mSATA Pin Assignments and Pin Type

The signal/pin assignments and descriptions are listed in Table 3-5.

Table 3-5. mSATA Pin Assignments and Pin Type

Pin #	Assignment	Description	Pin #	Assignment	Description
1	N/A	N/A	27	GND	Return Current Path
2	+3.3V	3.3V source	28	N/A	N/A
3	N/A	N/A	29	GND	Return Current Path
4	GND	Return Current Path	30	N/A	N/A
5	N/A	N/A	31	Rx-	SATA Differential
6	N/A	N/A	32	N/A	N/A
7	N/A	N/A	33	Rx+	SATA Differential
8	N/A	N/A	34	GND	Return Current Path
9	GND	Return Current Path	35	GND	Return Current Path
10	N/A	N/A	36	Reserved	No Connect
11	N/A	N/A	37	GND	Return Current Path
12	N/A	N/A	38	Reserved	No Connect
13	N/A	N/A	39	+3.3V	3.3V source
14	N/A	N/A	40	GND	Return Current Path
15	GND	Return Current Path	41	+3.3V	3.3V source
16	N/A	N/A	42	N/A	N/A
17	N/A	N/A	43	GND	Return Current Path
18	GND	Return Current Path	44	N/A	N/A
19	N/A	N/A	45	Reserved	N/A
20	N/A	N/A	46	N/A	N/A
21	GND	Return Current Path	47	Reserved	N/A
22	N/A	N/A	48	N/A	N/A
23	Tx+	SATA Differential	49	DA/DSS	Device Activity / Disable Staggered Spin Up
24	+3.3V	3.3V source	50	GND	Return Current Path
25	Tx-	SATA Differential	51	Presence Detection	Shall be pulled to GND by device
26	GND	Return Current Path	52	+3.3V	3.3V source

3.2. Electrical Specifications

The following table defines all D.C. Characteristics for the mSATA products. Unless otherwise stated, conditions are:

Vcc = 3.3V ± 5%

Ta = -45°C to 90°C

3.2.1. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Storage Temperature	Ts	-65	+150	°C
Operating Temperature	T_A	-45	+90	°C
Vcc with respect to GND	Vcc	-0.3	3.6	V

3.2.2. DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	Vin	-0.5	Vcc + 0.5	V
Output Voltage	Vout	-0.3	Vcc + 0.3	V
Input Leakage Current	I_{LI}	-10	10	uA
Output Leakage Current	I_{LO}	-10	10	uA
Input/Output Capacitance	C_I/C_o		10	pF
Operating Current	I_{CC}			mA
Sleep Mode			80	
Active			270	

3.2.3. AC Characteristics

Cactus Technologies® mSATA products conforms to all AC timing requirements as specified in the Serial ATA v2.6 specifications. Please refer to that document for details of AC timing for all operation modes of the device.

4. ATA Drive Register Set Definition and Protocol

The communication to or from the mSATA SSD is done using FIS. Legacy ATA protocol is supported by using the legacy mode defined in the SATA specifications. In this mode, the FIS has defined fields which provide all the necessary ATA task file registers for control and status information. The Serial ATA interface does not support Primary/Secondary or Master/Slave configurations. Each SATA channel supports only one SATA device, with the register selection as defined by the ATA standard.

4.1. ATA Task File Definitions

The following sections describes the usage of the ATA task file registers. Note that the Alternate Status Register of legacy ATA is not defined for SATA drives.

4.1.1. Data Register

The Data Register is a 16-bit register, and it is used to transfer data blocks between the SSD data buffer and the Host.

4.1.2. Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

4.1.3. Feature Register

This register provides information regarding features of the SSD that the host can utilize.

4.1.4. Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the SSD. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

4.1.5. Sector Number (LBA 7-0) Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any SSD data access for the subsequent command.

4.1.6. Cylinder Low (LBA 15-8) Register

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

4.1.7. Cylinder High (LBA 23-16) Register

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

4.1.8. Drive/Head (LBA 27-24) Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.
Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.
Bit 5 This bit is set to 1.
Bit 4 (DRV) DRV is the drive number. This should always be set to 0.
Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

4.1.9. Status Registers

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the device has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the device is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the device is ready.

Bit 3 (DRQ) The Data Request is set when the device requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

4.1.10. Device Control Register

This register is used to control the drive interrupt request and to issue an ATA soft reset to the drive. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
HOB	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is used in 48-bit addressing mode. When cleared, the host can read the most recently written values of the Sector Count,Drive/Head and LBA registers. When set, the host will read the previous written values of these registers. A write to any Command block register will clear this bit.

Bit 6 This bit is an X (Do not care).

Bit 5 This bit is an X (Do not care).

Bit 4 This bit is an X (Do not care).

Bit 3 This bit is ignored by the drive.

Bit 2 (SW Rst) This bit is set to 1 in order to force the drive to perform an AT Disk controller Soft Reset operation. The drive remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the drive are disabled. This bit is set to 0 at power on and Reset.

Bit 0 This bit is ignored by the drive.

4.1.11. Drive Address Register

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.
Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the SSD. Following are some possible solutions to this problem:

1. Locate the SSD at a non-conflicting address (i.e., Secondary address (377) when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and a SSD in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a SSD product is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the SSD's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the SSD or b) if provided use an additional Primary/Secondary configuration in the SSD that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

5. ATA Command Description

This section defines the ATA command set supported by the Cactus Technologies® mSATA SSD.

5.1. ATA Command Set

Table 5-6 summarizes the supported ATA command set .

Table 5-6. ATA Command Set

COMMAND	Code	FR	SC	SN	CY	DH
Check Power Mode	E5h, 98h	-	-	-	-	D
Data Set Management	06h	-	Y	-	-	D
Download Microcode	92h	Y	Y	Y	-	D
Execute Drive Diagnostic	90h	-	-	-	-	-
Flush Cache	E7h	-	-	-	-	D
Flush Cache Ext	EAh	-	-	-	-	D
Format Track	50h	-	Y	-	Y	Y
Identify Drive	ECh	-	-	-	-	D
Idle	E3h, 97h	-	Y	-	-	D
Idle Immediate	E1h, 95h	-	-	-	-	D
Media Lock	DEh	-	-	-	-	D
Media Unlock	DFh	-	-	-	-	D
NOP	00h	-	-	-	-	D
Read Buffer	E4h	-	-	-	-	D
Read DMA	C8h, C9h	-	Y	Y	Y	Y
Read DMA Ext	25h	-	Y	Y	Y	D
Read FPDMA Queued	60h	Y	Y	Y	Y	Y
Read Log Ext	2Fh	-	Y	Y	Y	D
Read Multiple	C4h	-	Y	Y	Y	Y

COMMAND	Code	FR	SC	SN	CY	DH
Read Multiple Ext	29h	-	Y	Y	Y	D
Read Native Max Address	F8h	-	-	-	-	D
Read Native Max Address Ext	27h	-	-	-	-	D
Read Sector(s)	20h, 21h	-	Y	Y	Y	Y
Read Sector(s) Ext	24h	-	Y	Y	Y	D
Read Verify Sector(s)	40h, 41h	-	Y	Y	Y	Y
Read Verify Sector(s) Ext	42h	-	Y	Y	Y	D
Recalibrate	1Xh	-	-	-	-	D
Security Disable Password	F6h	-	-	-	-	D
Security Erase Prepare	F3h	-	-	-	-	D
Security Erase Unit	F4h	-	-	-	-	D
Security Freeze Lock	F5h	-	-	-	-	D
Security Set Password	F1h	-	-	-	-	D
Security Unlock	F2h	-	-	-	-	D
Seek	7Xh	-	-	Y	Y	Y
Set Features	EFh	Y	-	-	-	D
Set Max Address	F9h	-	Y	Y	Y	Y
Set Max Address Ext	37h	-	Y	Y	Y	D
Set Multiple Mode	C6h	-	Y	-	-	D
Set Sleep Mode	E6h, 99h	-	-	-	-	D
SMART	B0h	Y	Y	-	Y	D
Stand By	E2h, 96h	-	-	-	-	D
Stand By Immediate	E0h, 94h	-	-	-	-	D
Write Buffer	E8h	-	-	-	-	D
Write DMA	Cah, CBh	-	Y	Y	Y	Y
Write DMA Ext	35h	-	Y	Y	Y	D
Write FPDMA Queued	61h	Y	Y	Y	Y	D
Write Multiple	C5h	-	Y	Y	Y	Y
Write Multiple Ext	39h	-	Y	Y	Y	D
Write Sector(s)	30h, 31h	-	Y	Y	Y	Y
Write Sector(s) Ext	34h	-	Y	Y	Y	D
Write Verify	3Ch	-	Y	Y	Y	Y

Definitions: FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Drive/Drive/Head Register.
Y—The register contains a valid parameter for this command. For the Drive/Head Register Y means both the drive and head parameters are used; D—only the drive parameter is valid and not the head parameter.

Note: 1. For SATA drives, the drive number is always 0.

5.1.1. Identify Drive—ECH

The Identify Drive command enables the host to receive parameter information from the drive. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 5-7. All reserved bits or words are zero. Table 5-7 is the definition for each field in the Identify Drive Information.

Table 5-7. Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	045AH	2	General configuration bit-significant information.
1	XXXXH	2	Default number of cylinders; capacity dependent.

Word Address	Default Value	Total Bytes	Data Field Type Information
2	0000H	2	Reserved.
3	00XXH	2	Default number of heads; capacity dependent.
4	0000H	2	Number of unformatted bytes per track.
5	0200H	2	Number of unformatted bytes per sector.
6	XXXXH	2	Default number of sectors per track; capacity dependent.
7-8	XXXXH,XXXXH	4	Number of sectors per drive (Word 7 = MSW, Word 8 = LSW); capacity dependent.
9	0000H	2	Reserved.
10-19	aaaa	20	Serial number in ASCII (Right Justified).
20	0002H	2	Buffer type (dual ported multi-sector)
21	0001H	2	Buffer size in 512 bytes increments
22	0004H	2	# of ECC bytes passed in R/W Long commands
23-26	aaaa	8	Firmware revision in ASCII . Big Endian Byte Order in Word.
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word.
47	8001H	2	Maximum number of sectors on Read/Write Multiple command: 1
48	0000H	2	Double Word not supported.
49	0F00H	2	Capabilities: DMA, LBA, IORDY supported
50	4001H	2	Capabilities: device specific standby timer minimum
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	Single Word DMA data transfer cycle timing mode (not supported).
53	0007H	2	Data fields 54-58,64-70 and 88 are valid.
54	XXXX	2	Current numbers of cylinders.
55	XXXX	2	Current numbers of heads.
56	XXXX	2	Current sectors per track.
57-58	XXXX	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW).
59	010XH	2	Multiple sector setting is valid; low byte is capacity dependent.
60-61	XXXX	4	Total number of sectors addressable in LBA Mode.
62	0000H	2	Single Word DMA transfer not implemented
63	0X07H	2	Multiword DMA modes 0-2 are supported; upper byte reflects currently selected MWDMA mode.
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum MWDMA cycle time per word is 120ns.
66	0078H	2	Recommended MWDMA cycle time is 120ns.
67	0078H	2	Minimum PIO cycle time without IORDY flow control is 120ns.
68	0078H	2	Minimum PIO cycle time with IORDY flow control is 120ns.
69	8000H	2	CFast specification supported
70-74	0000H	10	Reserved
75	001FH	2	Queue depth of 32 for NCQ
76	0306H	2	Supports SATA NCQ, Gen 1, Gen2 signaling rates, host initiated power management requests
77-79	0000H	6	Reserved
80	01E0H	2	Supports ATA5 to ATA8 standard.
81	FFFFH	2	No minor revision reported.
82	742BH	2	Command set: NOP, READ BUFFER, WRITE BUFFER, HPA, volatile write cache, power management feature set, Security Mode feature set, SMART feature set
83	7401H	2	48-bit mode supported; Flush Cache/Flush Cache Ext, LAB48, microcode download supported.
84	4120H	2	World wide name, general purpose logging supported
85	74XXH	2	Feature status
86	B401H	2	Feature status
87	4120H	2	Feature status
88	XX7FH	2	UDMA Modes 0-6 supported.
89	0000H	2	Time for Security Erase Unit not specified.
90	0000H	2	Time for Enhanced Security Erase Unit not specified.
91	0000H	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
92	XXXXH	2	Master password revision code
93-99	0000H	14	Reserved
100-103	XXXXH	8	Maximum user LBA for 48-bit addressing mode.
104	0000H	2	Reserved
105	0001H	2	# of sectors per Data Set Management command.
106-107	0000H	4	Reserved
108-111	XXXXH	8	Word Wide Name
112-118	0000H	14	Reserved
119	4000H	2	Command/Feature set supported extension.
120	4000H	2	Command/Feature set enabled extension.
121-127	0000H	14	Reserved
128	0XXXH	2	Security status
129	XX00H	2	Write Protect status: Bit 15: Permanent write protect, out of spare blocks Bit 14: Permanent write protect due to corrupted tables Bit 13: read protection due to table corruption Bit 9: Permanent write protect due to vendor command Bit 8: Temporary write protect due to vendor command
130-133	aaaa	8	Firmware date string
134-135	XXXXH	4	Obsolete
136-141	aaaa	12	Firmware file name
142-147	aaaa	12	Preformat file name
148-153	aaaa	12	Anchor program file name
154-158	0000H	10	Reserved
159	A2XXH	2	Controller major and minor revisions
160	80FAH	2	CFA Power mode: no level 1, max. 250mA
161	8001H	2	CFast specific support: not relevant for mSATA
162	0000H	2	CPRM not supported
163	0000H	2	CFA Advanced modes: not relevant for mSATA
164	0000H	2	CFA Advnaced modes: not relevant for mSATA
165-168	0000H	8	Reserved
169	0001H	2	TRIM bit in Data Set Management supported
170-216	0000H	94	Reserved
217	0001H	2	Solid State Device
218-221	0000H	8	Reserved
222	101FH	2	Transport major version: Serial ATA 2.6
223	FFFFH	2	Transport minor version not supported
224-254	0000H	62	Reserved
255	XXA5H	2	Integrity word

6. S.M.A.R.T. Support

Cactus Technologies® -900 Series mSATA SSDs support S.M.A.R.T. Status and attribute reporting functions as determined by the value of the Feature Register. The S.M.A.R.T. sub-commands supported are as follows:

Code	Sub Command
D0	Read Data
D1	Read Attribute Thresholds
D2	Enable/Disable Attribute Autodave

Code	Sub Command
D5	Read Log
D6	Write Log
D8	Enable Operations
D9	Disable Operations
DA	Return Status
E0	Read Remap Data
E1	Read Wear Level Data

The general format for issuing a SMART command is as follows:

Register	7	6	5	4	3	2	1	0
Feature	Subcommand code							
Sector Count								
Sector Number								
Cyliner Low	4Fh							
Cylinder High	C2h							
Drive/Head	1	1	1	D				
Command	B0h							

6.1. S.M.A.R.T. Enable Operations

Enables the SMART function. This setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters.

6.2. S.M.A.R.T. Disable Operations

Disables the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on. Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error.

This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles.

6.3. S.M.A.R.T. Enable/Disable Attribute Autosave

This subcommand is issued with the Sector Count register set to either 00h or F1h. 00h enables Autosave while F1h disables it. However, this is in affect a NOP as the SMART attributes are always auto-saved.

6.4. S.M.A.R.T. Read Data

This subcommand returns 512 bytes of S.M.A.R.T. data structure. When this subcommand is issued, the Feature Register must contain D0h, the LBA Mid register must contain 4Fh and the LBA high register must contain C2h. The returned data has the following structure:

Byte	Value	Description
0-1	0010h	SMART structure revision number
2-361		1st – 30th attribute data (12 bytes each)
362	00h	Offline data collection status (no offline data collection)
363		Selftest execution status
364-365	0000h	Total time in seconds to complete offline data collection
366	00h	Reserved
367	00h	Offline data collection capability (no offline data collection)
368-369	0003h	S.M.A.R.T. Capability
370	00h	Error logging capability (no error logging capability)
371	00h	Reserved
372	00h	Short self-test routine recommended polling time
373	00h	Extended self-test routine recommended polling time
374-385	00h	Reserved
386-387	0004h	SMART Hyperstone structure version
388-391		Firmware “Commit” counter
392-395		Firmware Wear Level Threshold
396		“1” : Global Wear Leveling active
397		“1” : Global Bad Block Management active
398-401		Average Flash Block Erase Count
402-405		Number of Flash Blocks involved in Wear Leveling

Byte	Value	Description
406-510	00h	Reserved
511		checksum

6.5. S.M.A.R.T. Attributes

The -900 series mSATA SSD monitors 10 attributes as shown in the following table:

ID	Description
196	Spare block count
213	Spare block count worse chip
229	Erase count
203	ECC error count
204	Corrected ECC error count
199	UDMA CRC error count
232	Number of reads
12	Power on count
241	Total LBAs written
242	Total LBAs read

The following tables lists the returned data for each reported attribute.

Attribute 196: Spare Block Count		
Byte	**Value**	**Description**
0	196	Attribute ID
1-2	0003h	Flags – Pre-fail type, attribute value is updated during normal operation
3		Attribute value – percentage of remaing spare blocks summed over all the flash chips (100 x current spare blocks / initial spare blocks)
4		Attribute value (worst value)
5-7		Sum of the initial spare blocks over all flash chips
8-10		Sum of the current spare blocks over all flash chips
11	00h	Reserved

Attribute 213: Spare Block Count Worst Chip Threshold		
Byte	**Value**	**Description**
0	213	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	This value is fixed at 100.
4	64h	Attribute value (worse value).
5-7		Initial number of spare blocks of the flash chip with the worse current spare block count.
8-10		Current number of spare blocks of the flash chip with the worse current spare block count.
11	00h	Reserved

Attribute 229: Erase Count		
Byte	**Value**	**Description**
0	229	Attribute ID
1-2	000Xh	Flags – Pre-fail or Advisory type, attribute value is updated during normal operation
3		Attribute value. The value is the estimate of the percentage of remaining life based on the number of block erases compared to the target erase cycles per flash block.
4		Attribute value (worse value)
5-10		Estimated total number of block erases
11		Reserved

Attribute 203 : Total ECC Error Count		
Byte	**Value**	**Description**
0		Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of ECC errors (correctable and uncorrectable)
9-10		--
11	00h	Reserved

Attribute 204 : Correctable ECC Error Count		
Byte	**Value**	**Description**
0	204	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of correctable ECC errors.
9-10		--
11	00h	Reserved

Attribute 199 : UDMA ECC Error Count		
Byte	**Value**	**Description**
0	199	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of UDMA ECC errors.
9-10		--
11	00h	Reserved

Attribute 232 : Total number of reads		
Byte	**Value**	**Description**
0	232	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-10		Total number of flash read commands.
11	00h	Reserved

Attribute 12 : Power On Count		
Byte	**Value**	**Description**
0	12	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of power on cycles.
9-10		--
11	00h	Reserved

Attribute 241 : Total LBAs Written (in units of 32MB)		
Byte	**Value**	**Description**
0	241	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-10		Total number of LBAs written, divided by 65536.
11	00h	Reserved

Attribute 242 : Total LBAs Read (in units of 32MB)		
Byte	**Value**	**Description**
0	242	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-10		Total number of LBAs read, divided by 65536.
11	00h	Reserved

6.6. S.M.A.R.T. Read Attribute Thresholds

This command returns one sector of SMART attribute threshold data; the format is as follows:

Byte	Value	Description
0-1	0010h	SMART structure version
2-361		Attribute threshold entries 1-30 (12 bytes each)
362-379	00h	Reserved
380-510	00h	--
511		Checksum

The thresholds reported are as follows:

Byte	Value	Description
0	196	Attribute ID – Spare Block Count
1		Spare block count threshold as defined during pre-format
2-11	00h	Reserved

Byte	Value	Description
0	213	Attribute ID – Spare Block Count Worse Chip
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	229	Attribute ID – Erase Count
1		Erase count threshold as defined during pre-format
2-11	00h	Reserved

Byte	Value	Description
0	203	Attribute ID – Total ECC Errors
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	204	Attribute ID – Correctable ECC Errors
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	199	Attribute ID – UDMA CRC Errors
1	00h	No threshold defined for this threshold.
2-11	00h	Reserved

Byte	Value	Description
0	232	Attribute ID – Total number of reads
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	12	Attribute ID – Power on count
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	241	Attribute ID – Total LBAs written
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	242	Attribute ID – Total LBAs read
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

6.7. S.M.A.R.T. Return Status

Reports the drive reliability status. Values reported when a predicted defect has not been detected:

Cylinder Low register: 4Fh
Cylinder High register: C2h

Values reported when a predicted defect has been detected:

Cylinder Low register: F4h
Cylinder High register: 2Ch

6.8. S.M.A.R.T. Read Log

This command returns the data of the SMART log. When issuing this command, set the Sector Count register to the number of sectors to read and set the Sector Number register to the Log address. The Log addresses are defined as follows:

Address	Description
0x00	Log directory
0x10	NCQ Command error log
0x80-0x9F	Host Vendor Specific logs
0xA0	SMART Wear Level data
0xA1	SMART Remap data
0xA2	Reserved
0xA3	Reserved

The Log directory (address 0) returns 1 sector of data that shows the number of sectors for the defined Log addresses:

Byte	Value	Description
0-1	1	SMART logging version
2-19	0	Reserved
20-21	1	Number of sectors for SMART Log at address 0x10
22-255	0	Reserved
256-319	16	Number of sectors for SMART Log at addresses 0x80-0x9F
320-321	4	Number of sectors for SMART Log at address 0xA0
322-323	1	Number of sectors for SMART Log at address 0xA1

Byte	Value	Description
324-325	1	Number of sectors for SMART Log at address 0xA2
326-327	1	Number of sectors for SMART Log at address 0xA3
328-511	0	Reserved

The NCQ Command Error Log returns information about the most recent NCQ command failure. The Host Vendor Specific Logs can be used by the host to store and retrieve arbitrary data. The SMART Wear Level Data and SMART Remap Data logs return the same data that is also returned by the SMART A2 Read Wear Level Data and SMART A2 Read Remap Data commands.

6.9. S.M.A.R.T. Write Log

This command writes data of the SMART log. When issuing this command, set the Sector Count register to the number of sectors to write and set the Sector Number register to the Log address. Only the Host Vendor Specific logs can be written, all other logs are read only.

6.10. S.M.A.R.T. Read Remap Data

This command returns spare block information. When issuing this command, set the Sector Count register to 1. The information returned is the number of initial spare blocks per flash chip and the current number of spare blocks per flash chip. The format is as follows:

Bytes	Description
0-31	Initial number of spare blocks for flash chip 0 to 15 (2 bytes per chip)
32-63	Current number of spare blocks for flash chip 0 to 15 (2 bytes per chip)
64-511	Reserved

6.11. S.M.A.R.T. Read Wear Level Data

This command returns 4 sectors of wear level information. When issuing this command, set the Sector Count register to 4. The information returned is the distribution of blocks in each of 1024 wear level classes. For each class, the entry contains the number of blocks in that class. The format of the returned data is as follows, where n denotes the sector number from 0 to 3:

Bytes	Description
0-1	Number of blocks in wear level class 256*n + 0
2-3	Number of blocks in wear level class 256*n + 1

Bytes	Description
508-509	Number of blocks in wear level class 256*n + 254
510-511	Number of blocks in wear level class 256*n + 255

Thus, the first sector (n= 0) returns information about wear level class 0 to 255. The 2nd sector (n= 1) returns information about wear level class 256 to 511, and so on. A block moves from one wear level class to the next once it had reached the 'Wear Level Threshold' specified during pre-format.

Appendix A. Ordering Information

Model KDXFY-900SM

Where: X is drive capacities:

4G ---------- 4GB
8G ---------- 8GB
16G ---------- 16GB
32G ---------- 32GB
64G ---------- 64GB
128G ---------- 128GB*

**** special order only, extra lead time required; check with Cactus Technologies® sales for details***

Where Y is temperature:
Blank ---------- Standard temperature (0° C to +70° C)
I ---------- Extended temperature (-45° C to +90° C)

Where M is lid option:
M1 ---------- no lid
M2 ---------- with lid

Example:

(1) 8GB mSATA ---------- KD8GF-900SM1
(2) 8GB mSATA Extended Temp ---------- KD8GFI-900SM1
(3) 8GB mSATA with lid ---------- KD8GF-900SM2

Appendix B.Technical Support Services

B.1.Direct Cactus Technologies® Technical Support

Email: tech@cactus-tech.com

Appendix C.Cactus Technologies® Worldwide Sales Offices

Email: sales@cactus-tech.com

Email: americas@cactus-tech.com

Appendix D.Limited Warranty

I. WARRANTY STATEMENT

Cactus Technologies® warrants its Industrial Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for five years from the date of purchase. This express warranty is extended by Cactus Technologies® Limited to customers of our products.

II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies® responsibilities regarding the Cactus Technologies® Industrial Grade Flash Storage Products. Cactus Technologies®, at its sole option, will repair, replace or refund the purchase price of the defective product. Cactus Technologies® guarantees our products meet all specifications detailed in our product manuals. Although Cactus Technologies® products are designed to withstand harsh environments and have the highest specifications in the industry, they are not warranted to never have failure and Cactus Technologies® does not warranty against incidental or consequential damages. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or backup features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within five years of purchase, Cactus Technologies® will have the option of repairing, replacing or refunding the purchase price the defective product, if the following conditions are met:

A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.

B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty shall be tested to the product’s functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs. Cactus Technologies® Limited may repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

IV. RECEIVING WARRANTY SERVICE

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies® Limited. Please contact Cactus Technologies® Customer Service department (tech@cactus-tech.com) with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies® will issue a Return Material Authorization or Product Repair Authorization number with shipping instructions.