-503 Series
Industrial Grade SSD
Product Manual

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1.Introduction to Cactus Technologies® -503 Series Industrial Grade SSD Products

Features:

- Solid state design with no moving parts
- Industry standard 2.5” IDE Drive form factor
- Supports ATA PIO Modes 0-6
- Supports MWDMA Modes 0-4
- Supports UDMA Modes 0-6
- Supports ATA S.M.A.R.T Feature Set
- Supports ATA Security Feature Set
- High reliability, MTBF > 4,000,000 hrs.
- Enhanced error correction, < 1 error in 10^{14} bits read
- Intelligent power management to reduce power consumption
- Dual voltage support: 3.3V/5.0V

Cactus Technologies® Solid State Drive(SSD) is a high capacity solid-state flash memory product that complies with the ANSI ATA standard and is electrically compatible with an IDE disk drive. Cactus Technologies® SSDs provide up to 128GB of formatted storage capacity in 2.5”form factors.

Cactus Technologies® Industrial Grade SSD products use high quality flash memory from well known vendors, such as Toshiba Corporation. In addition, it includes an on-drive intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control.

1.1. Supported Standards

Cactus Technologies® SSD is fully electrically compatible with the following specification:

- ATA 7 Specification published by ANSI: X3.221 AT Attachment Interface for Disk Drives

1.2. Product Features

Cactus Technologies® Industrial SSD contains a high level, intelligent controller. This intelligent controller provides many capabilities including the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

1.2.1. Host and Technology Independence

Cactus Technologies® Industrial SSD appears as a standard ATA disk drive to the host system. The drive utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the drive as per the ATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the drive. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support the Cactus Technologies® Industrial SSD products today will continue to work with future Cactus Technologies® Industrial SSDs built with new flash technology without having to update or change host software.

1.2.2. Defect and Error Management

Cactus Technologies® Industrial SSD contains a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies® Industrial SSDs is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the drive has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies® Industrial SSDs unparalleled reliability.

1.2.3. Power Supply Requirements

Cactus Technologies® Industrial SSD is a dual voltage product, which means it will operate at a voltage range of 3.30 volts ±10% or 5.00 volts ± 10%.

2.Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. Environmental Specifications

		Cactus Technologies® SSD
Temperature	Operating:	0° C to +70° C (Standard) -45° C to +90° C (Extended)
Humidity	Operating & Non-Operating:	8% to 95%, non-condensing
Acoustic Noise		0 dB
Vibration	Operating & Non-Operating:	20 G MIL-STD-883G Method 2005.2 condition A
Shock	Operating & Non-Operating:	3,000 G MIL-STD-883G Method 2002.3 condition C
Altitude (relative to sea level)	Operating & Non-Operating:	100,000 feet maximum

2.2. System Power Requirements

Table 2-2. Power Requirements

		Cactus Technologies® Industrial SSD
DC Input Voltage (VCC) **100 mV max. ripple (p-p)**		5V ±10%
(Maximum Average Value) **See Notes.**	Sleep: Reading: Writing:	15 mA 145 mA 100 mA

NOTES: All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all drive inputs are static CMOS levels and in a “Not Busy“ operating state.

2.3. System Performance

All performance timings assume the drive controller is in the default (i.e., fastest) mode.

Table 2-3. Performance

Read Transfer Rate		Up to 50.0 MBytes/ sec
Write Transfer Rate		Up to 25.0 MBytes/ sec

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2.4. System Reliability

Table 2-4. Reliability

Data Reliability	< 1 non-recoverable error in 10^{14} bits READ
Endurance (estimated TBW):	
1GB	60TB
2GB	120TB
4GB	240TB
8GB	480TB
16GB	960TB
32GB	1920TB
64GB	3840TB
128GB	7680TB

Note: TBW is estimated based on a workload of sequential, large block writes.

2.5. Physical Specifications

The following sections provide the physical specifications for Cactus Technologies® Industrial SSD products.

2.5.1. 2.5” SSD Physical Specifications

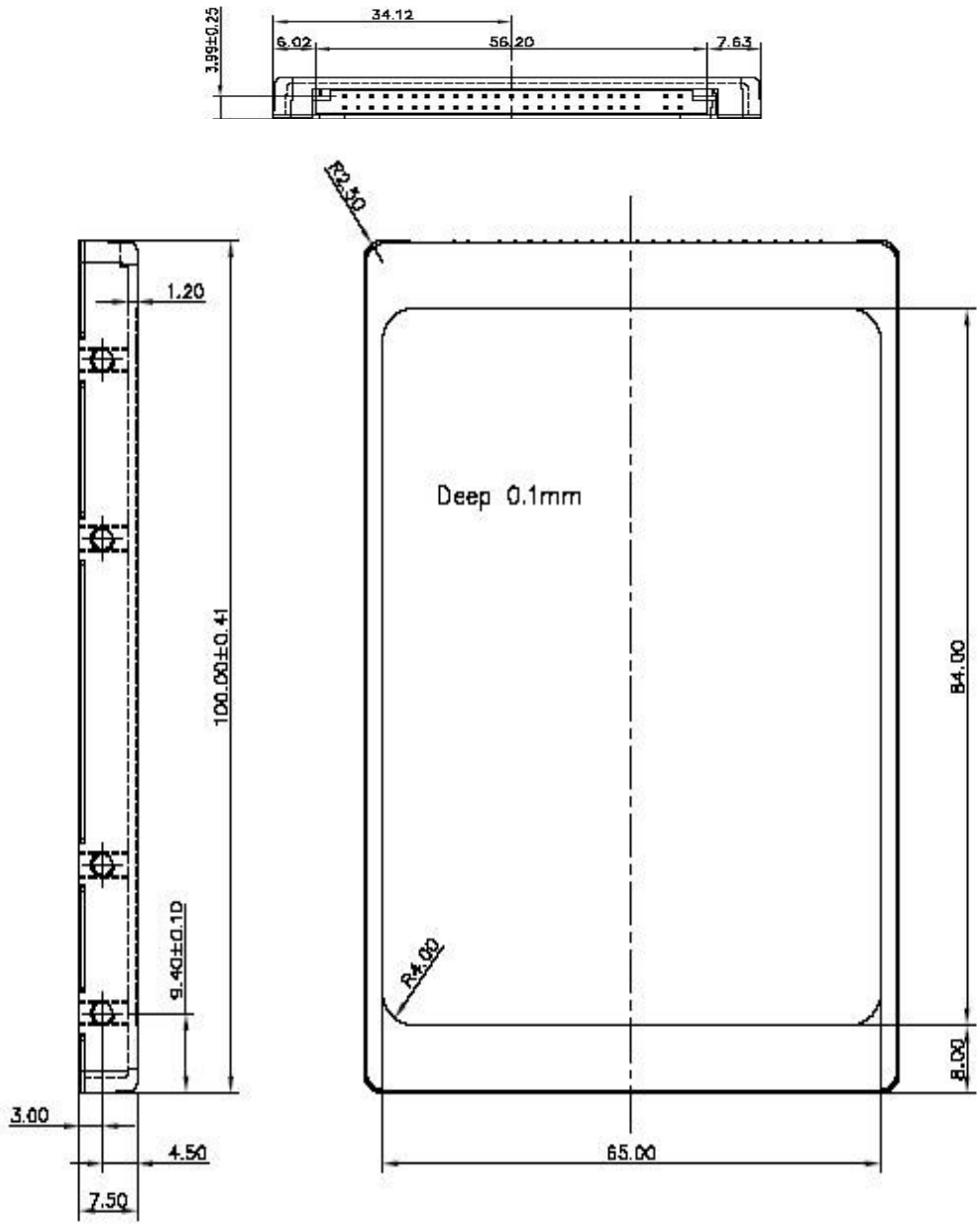

Figure 2-1. 2.5” SSD Dimensions

2.5.2. Capacities

Cactus Technologies® -503 series industrial grade SSD is available in 1,2,4,8,16,32,64 and 128GB.

3. Interface Description

The following sections provide detailed information on the Cactus Technologies® Industrial SSD interface.

3.1. SSD Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 3-5. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Sections 3.3.1 to 3.3.4 define the DC characteristics for all input and output type structures.

Table 3-5. SSD Pin Assignments and Pin Type

Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type
1	-Reset	I	2	GND	
3	Data 7	I/O	4	Data 8	I/O
5	Data 6	I/O	6	Data 9	I/O
7	Data 5	I/O	8	Data 10	I/O
9	Data 4	I/O	10	Data 11	I/O
11	Data 3	I/O	12	Data 12	I/O
13	Data 2	I/O	14	Data 13	I/O
15	Data 1	I/O	16	Data 14	I/O
17	Data 0	I/O	18	Data 15	I/O
19	GND		20	Key	
21	-DMARQ	O	22	GND	
23	-IOW/STOP	I	24	GND	
25	-IOR/ -HDMARDY/ HSTROBE	I	26	GND	
27	IORDY/ -DDMARDY/ DSTROBE	O	28	-CSEL	I
29	-DMACK	I	30	GND	
31	IRQ	O	32	(reserved)	
33	A1	I	34	-PDIAG	I/O
35	A0	I	36	A2	I
37	-CS0	I	38	-CS1	I
39	-DASP	I/O	40	GND	
41	Vcc		42	Vcc	
43	GND		44	Reserved	

3.2. Signal Description

Table 3-6 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the SSD sources are outputs. The SSD logic levels conform to those specified in the *ANSI ATA Specification*.

Table 3-6. Signal Description

Signal Name	Dir.	Description
A2—A0	I	A[2:0] is used to select the one of eight registers in the Task File.
-PDIAG	I/O	This input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
-DASP	I/O	This input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CS0, -CS1	I	-CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL	I	This internally pulled up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15—D00	I/O	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. All Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bits using D00-D15.
GND	--	Ground.
-IORD/-HDMARDY/ HSTROBE	I	This is an I/O Read strobe generated by the host for PIO data-in and register transfers. Data is latched by the host on the rising edge of this signal. -HDMARDY is a flow control signal for UDMA data-in transfers. This signal is asserted by the host to indicate to the device that it is ready to accept data. The host may negate this signal to pause the trasnfer. HSTROBE is a strobe signal generated by the host for UDMA data-out transfers. Data is transferred on both edges of this signal.
-IOWR/STOP	I	The I/O Write strobe pulse is used to clock I/O data on the Data bus into the SSD for PIO data-out and register transfers. Data is latched by the device on the rising edge of this signal. In UDMA transfers, STOP is asserted by the host to signal the termination of the UDMA burst.
INTRQ	O	This signal is the active high Interrupt Request to the host.
-RESET	I	This input pin is the active low hardware reset from the host.
VCC	--	+5 V, +3.3 V power.
-IORDY/-DDMARDY/ DSTROBE	O	The -**IORDY** signal is driven by the SSD to extend the I/O cycle in progress for PIO modes 3 and above. -DDMARDY is a flow control signal for UDMA data-out transfers. This signal is asserted by the device to signal to the host that it is ready to accept data. The device may negate this signal to pause the transfer. DSTROBE is a data strobe signal generated by the device for UDMA data-in transfers. Data is transferred on both edges of this signal.
DMARQ	O	This signal is generated by the device to request MWDMA or UDMA transfers.
-DMACK	I	This signal is asserted by the host to acknowledge a DMARQ from the device.

3.3. Electrical Specification

The following table defines all D.C. Characteristics for the SSD Series. Unless otherwise stated, conditions are:

Vcc = 5V ± 10% or Vcc = 3.3V ± 10%
Ta = -45°C to 90°C

3.3.1. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Storage Temperature	Ts	-65	+150	ºC
Operating Temperature	T_A	-45	+90	ºC
Vcc with respect to GND	Vcc	-0.3	6.5	V

3.3.2. DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	Vin	-0.5	Vcc + 0.5	V
Output Voltage	Vout	-0.3	Vcc + 0.3	V
Input Leakage Current	I_{LI}	-10	10	uA
Output Leakage Current	I_{LO}	-10	10	uA
Input/Output Capacitance	C_I/C_o		10	pF
Operating Current Sleep Mode Active	I_{CC}		 15 150	mA

3.3.3. AC Characteristics

Cactus Technologies® SSD products conforms to all AC timing requirements as specified in the ANSI ATA specifications. Please refer to that document for details of AC timing for all operation modes of the device.

3.4. I/O Transfer Function

Table 3-7defines the function of the operations for the SSD.

Table 3-7. SSD I/O Function

Function Code	-CE2	-CE1	Address	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Do not care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Do not care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out

4.ATA Drive Register Set Definition and Protocol

The communication to or from the SSD is done using the Task File registers, which provide all the necessary registers for control and status information. The ATA interface connects peripherals to the host using four register mapping methods. Table 4-7 is a detailed description of these methods.

Table 4-7. I/O Configurations

Address	Drive #	Description
1F0-1F7, 3F6-3F7	0	Primary I/O Mapped Drive 0
1F0-1F7, 3F6-3F7	1	Primary I/O Mapped Drive 1
170-177, 376-377	0	Secondary I/O Mapped Drive 0
170-177, 376-377	1	Secondary I/O Mapped Drive 1

4.1. Task File Addressing

I/O decoding to access the task file registers is as listed in Table 4-8.

Table 4-8. Task File I/O Decoding

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0
1	0	0	0	0	RD Data	WR Data
1	0	0	0	1	Error Register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No./LBA low	Sector No./LBA low
1	0	1	0	0	Cylinder Low/LBA mid	Cylinder Low/ LBA mid
1	0	1	0	1	Cylinder High/LBA high	Cylinder High/LBA high
1	0	1	1	0	Select Drive/Head	Select Drive/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control
0	1	1	1	1	Drive Address	Reserved

4.2. ATA Registers

4.2.1. Data Register (Address—1F0[170]

The Data Register is a 16-bit register, and it is used to transfer data blocks between the SSD data buffer and the Host.

4.2.2. Error Register (Address—1F1[171]; Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

4.2.3. Feature Register (Address—1F1[171]; Write Only)

This register provides information regarding features of the SSD that the host can utilize.

4.2.4. Sector Count Register (Address—1F2[172])

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the SSD. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

4.2.5. Sector Number (LBA 7-0) Register (Address—1F3[173])

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any SSD data access for the subsequent command.

4.2.6. Cylinder Low (LBA 15-8) Register (Address—1F4[174])

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

4.2.7. Cylinder High (LBA 23-16) Register (Address—1F5[175])

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

4.2.8. Drive/Head (LBA 27-24) Register (Address 1F6[176])

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.

Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5 This bit is set to 1.

Bit 4 (DRV) This bit will have the following meaning. DRV is the drive number. When DRV=0, drive 0 is selected When DRV=1, drive 1 is selected.

Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

4.2.9. Status and Alternate Status Registers (Address 1F7[177] and 3F6[376])

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the device has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the device is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the device is ready.

Bit 3 (DRQ) The Data Request is set when the device requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

4.2.10. Device Control Register (Address—3F6[376])

This register is used to control the drive interrupt request and to issue an ATA soft reset to the drive. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
HOB	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is used in 48-bit addressing mode. When cleared, the host can read the most recently written values of the Sector Count,Drive/Head and LBA registers. When set, the host will read the previous written values of these registers. A write to any Command block register will clear this bit.

Bit 6 This bit is an X (Do not care).

Bit 5 This bit is an X (Do not care).

Bit 4 This bit is an X (Do not care).

Bit 3 This bit is ignored by the drive.

Bit 2 (SW Rst) This bit is set to 1 in order to force the drive to perform an AT Disk controller Soft Reset operation. The drive remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the drive are disabled. This bit is set to 0 at power on and Reset.

Bit 0 This bit is ignored by the drive.

4.2.11. Drive Address Register (Address 3F7[377])

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.
Implementation Note:
Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the SSD. Following are some possible solutions to this problem:

1. Locate the SSD at a non-conflicting address (i.e., Secondary address (377) when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and a SSD in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a SSD product is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the SSD's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the SSD or b) if provided use an additional Primary/Secondary configuration in the SSD that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

5.ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the Industrial SSD products. Commands are issued by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register.

5.1. ATA Command Set

Table 5-9 summarizes the supported ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 5-9. ATA Command Set

COMMAND	Code	FR	SC	SN	CY	DH	LBA
Check Power Mode	E5h or 98h	-	-	-	-	D	-
Execute Drive Diagnostic	90h	-	-	-	-	-	-
Data Set Management	06h	-	Y	-	-	D	-
Download Microcode	92h	Y	Y	Y	-	D	-
Flush Cache	E7h	-	-	-	-	D	-
Flush Cache Ext	EAh	-	-	-	-	D	-
Format Track	50h	-	Y	-	Y	Y	Y
Identify Drive	ECh	-	-	-	-	D	-
Idle	E3h or 97h	-	Y	-	-	D	-
Idle Immediate	E1h or 95h	-	-	-	-	D	-
Initialize Drive Parameters	91h	-	Y	-	-	Y	-
Media Lock	DEh	-	-	-	-	Y	-
Media Unlock	DFh	-	-	-	-	Y	-
NOP	00h	-	-	-	-	Y	-
Read Buffer	E4h	-	-	-	-	D	-
Read DMA	C8h or C9h	-	Y	Y	Y	Y	Y
Read DMA Ext	25h	-	Y	Y	Y	Y	Y
Read Log Ext	2Fh	-	Y	Y	Y	-	Y
Read Multiple	C4h	-	Y	Y	Y	Y	Y
Read Multiple Ext	29h	-	Y	Y	Y	Y	Y
Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
Read Sector(s) Ext	24h	-	Y	Y	Y	Y	Y
Read Verify Sector(s)	40h	-	Y	Y	Y	Y	Y
Read Verify Sector(s) Ext	42h	-	Y	Y	Y	Y	Y
Recalibrate	1Xh	-	-	-	-	D	-
Security Disable Password	F6h	-	-	-	-	D	-
Security Erase Prepare	F3h	-	-	-	-	D	-
Security Erase Unit	F4h	-	-	-	-	D	-
Security Freeze Lock	F5h	-	-	-	-	D	-
Security Set Password	F1h	-	-	-	-	D	-
Security Unlock	F2h	-	-	-	-	D	-
Seek	7Xh	-	-	Y	Y	Y	Y
Set Features	EFh	Y	-	-	-	D	-
Set Multiple Mode	C6h	-	Y	-	-	D	-
Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
SMART	B0h	Y	Y	-	Y	Y	-
Stand By	E2h or 96h	-	-	-	-	D	-
Stand By Immediate	E0h or 94h	-	-	-	-	D	-
Write Buffer	E8h	-	-	-	-	D	-

COMMAND	Code	FR	SC	SN	CY	DH	LBA
Write DMA	CAh or CBh	-	Y	Y	Y	Y	Y
Write DMA Ext	35h	-	Y	Y	Y	Y	Y
Write Log Ext	3Fh	-	Y	Y	Y	Y	Y
Write Multiple	C5h	-	Y	Y	Y	Y	Y
Write Multiple Ext	39h	-	Y	Y	Y	Y	Y
Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
Write Sectors(s) Ext	34h	-	Y	Y	Y	Y	Y
Write Verify Sector(s)	3Ch	-	Y	Y	Y	Y	Y

Definitions: FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Drive/Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use).

Y—The register contains a valid parameter for this command. For the Drive/Head Register Y means both the drive and head parameters are used; D—only the drive parameter is valid and not the head parameter.

5.1.1. Check Power Mode—98H, E5H

If the drive is in, going to, or recovering from the standby mode, the drive sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the drive is in active mode, the drive sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

5.1.2. Data Set Management—06H

This command performs a TRIM of the LBAs according to the transferred sectors.

5.1.3. Execute Drive Diagnostic—90H

The Executive Drive Diagnostic command performs the internal diagnostic tests implemented by the drive.

A code of 01h will be returned in the Error Register at the end of the command.

5.1.4. Format Track—50H

This command writes the desired head and cylinder of the selected drive with a vendor unique pattern. To remain host backward compatible, the drive expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the drive. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256).

5.1.5. Identify Drive—ECH

The Identify Drive command enables the host to receive parameter information from the drive. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 5-10. All reserved bits or words are zero. Table 5-10 is the definition for each field in the Identify Drive Information.

Table 5-10. Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	045AH	2	General configuration bit-significant information.
1	XXXXH	2	Default number of cylinders; capacity dependent.
2	0000H	2	Reserved.
3	00XXH	2	Default number of heads; capacity dependent.
4	0000H	2	Number of unformatted bytes per track.
5	0200H	2	Number of unformatted bytes per sector.
6	XXXXH	2	Default number of sectors per track; capacity dependent.
7-8	XXXXH,XXXXH	4	Number of sectors per drive (Word 7 = MSW, Word 8 = LSW); capacity dependent.
9	0000H	2	Reserved.
10-19	aaaa	20	Serial number in ASCII (Right Justified).
20	0002H	2	Buffer type (dual port).
21	0001H	2	Buffer size in 512 byte increments.
22	0004H	2	Number of ECC bytes passed on Read/Write Long Commands.
23-26	aaaa	8	Firmware revision in ASCII . Big Endian Byte Order in Word.
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word.
47	8001H	2	Maximum 1 sector on Read/Write Multiple command.
48	0000H	2	Double Word not supported.
49	0F00H	2	Capabilities: DMA Supported in True IDE mode (bit 8), LBA supported (bit 9).
50	4001H	2	Capabilities: device specific standby timer minimum.
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Single Word DMA data transfer cycle timing mode (not supported).
53	0007H	2	Data fields 54-58,64-70 and 88 are valid.
54	XXXX	2	Current numbers of cylinders.
55	XXXX	2	Current numbers of heads.
56	XXXX	2	Current sectors per track.
57-58	XXXX	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW).
59	010XH	2	Multiple sector setting is valid; low byte is capacity dependent.
60-61	XXXX	4	Total number of sectors addressable in LBA Mode.
62	0000H	2	Reserved
63	0X0XH	2	Multiword DMA modes supported; upper byte reflects currently selected MWDMA mode.
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum MWDMA cycle time per word is 120ns.
66	0078H	2	Recommended MWDMA cycle time is 120ns.
67	0078H	2	Minimum PIO cycle time without IORDY flow control is 120ns.
68	0078H	2	Minimum PIO cycle time with IORDY flow control is 120ns.
69-79	0000H	22	Reserved
80	01E0H	2	Supports ATA5 to ATA8 standard.
81	0000H	2	No minor revision reported.
82	702BH	2	Read/Write Buffer command supported; volatile write cache, power management feature set, Security Mode and SMART feature sets supported;
83	7401H	2	LBA48 supported; Flush Cache, Flush Cache Ext, Download Microcode supported.
84	4020H	2	General purpose logging supported
85	70XXH	2	Features enabled/disabled
86	3405H	2	Features enabled.
87	4020H	2	Features enabled.
88	XXXXH	2	UDMA Modes supported.
89	0000H	2	Time for Security Erase Unit not specified

Word Address	Default Value	Total Bytes	Data Field Type Information
90	0000H	2	Time for Enhanced Security Erase Unit not specified
91	0000H	2	Reserved
92	XXXXH	2	Master Password Revision Code
93	XXXXH	2	Hardware Reset Result
94-99	0000H	12	Reserved
100-103	XXXXH	8	Maximum user LBA for 48-bit addressing mode.
104	0000H	2	Reserved
105	0001H	2	Number of sectors per Data Set Management command
106-107	0000H	4	Reserved
108-111	0000H	8	World Wide Name
112-127	0000H	36	Reserved
128	0XXXH	2	Security Status
129	XX00H	2	Write Protect Status: bit 15 = permanent write protect, out of spare blocks Bit 14 = permanent write protect due to table corruption Bit 13 = read protection due to table corruption Bit 9 = permanent write protect from vendor command Bit 8 = temporary write protect from vendor command
130-133	XXXXH	8	Firmware date string
134	XXXXH	2	Reserved
135	045AH	2	General Configuration word for True-IDE mode
136-141	XXXXH	12	Firmware file name
142-147	XXXXH	12	Preformat file name
148-153	XXXXH	12	Anchor program file name
154-159	0000H	12	Reserved
160	XXXXH	2	Reserved
161	0000H	2	Reserved
162	0000H	2	Key Management Schemes: CPRM not supported
163	XXXXH	2	Reserved
164	XXXXH	2	Reserved
165-168	0000H	8	Reserved
169	0001H	2	Trim bit in Data Set Management supported
170-216	0000H	94	Reserved
217	0001H	2	Solid State Device (non-rotating media)
218-254	0000H	74	Reserved
255	XXA5H	2	Integrity word

5.1.6. Idle, Idle Immediate—97H, E3H, 95H, E1h

These commands cause the drive to go into idle mode.

5.1.7. Initialize Drive Parameters—91H

The Initialize Drive Parameters command causes the drive to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt. This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Drive/Head registers are used by this command. This command is obsolete in ATA5 but is supported for backwards compatibility.

5.1.8. Media Lock/Unlock—DEH, DFH

These commands are NOP.

5.1.9. Read Buffer—E4H

The Read Buffer command enables the host to read the current contents of the SSD's sector buffer. This command has the same protocol as the Read Sector(s) command.

5.1.10. Read DMA, Read DMA Ext—C8H, C9H, 25H

These commands read a number of sectors, as specified in the Sector Count register, in DMA mode

5.1.11. Read Log Ext—2FH

This command reads data from the general purpose log; the data read is described in the SMART log section.

5.1.12. Read Multiple, Read Multiple Ext—C4H,29H

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple, command.

5.1.13. Read Sector(s),Read Sector(s) Ext—20H, 21H, 24H

The Read Sector(s) command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the drive sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

5.1.14. Read Verify Sector(s), Read Verify Sector(s) Ext—40H, 42H

The Read Verify Sector(s) command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the drive sets BSY.

When the requested sectors have been verified, the drive clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

5.1.15. Recalibrate—1XH

The Recalibrate command is effectively a NOP command to the drive and is provided for compatibility purposes.

5.1.16. Security Disable Password -- F6H

This command checks and removes the Security Mode password.

5.1.17. Security Erase Prepare—F3H

This command is issued in preparation for the Security Erase Unit command.

5.1.18. Security Erase Unit—F4H

This command checks the Security Mode password and erases all user data on the device.

5.1.19. Security Freeze Lock—F5H

This command disables further Security Mode commands until the next hardware reset or power on.

5.1.20. Security Set Password—F1H

This command sets the Security Mode password.

5.1.21. Security Unlock—F2H

This command enables access to a Security Locked device.

5.1.22. Seek—7XH

The Seek command is effectively a NOP command to the drive although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

5.1.23. Set Features—EFH

The Set Features command is used by the host to establish or select certain features.

Table 5-11 defines all features that are supported.

Table 5-11. Features Supported

Feature	Operation
02H/82H	Enable/disable write cache (currently ignored as Write Caching is disabled at low level format)
03H	Set transfer mode.
05H/85H	Enable/disable advanced power management
09H/89H	Enable/disable extended power operations
0AH/8AH	Enable/disable power level 1 commands
55H/AAH	Disable/enable Read Look Ahead.
66H/CCH	Disable/enable Power on Reset (POR) establishment of defaults at Soft Reset.
69H	NOP; accepted for backward compatibility.
96H	NOP; accepted for backward compatibility.
97H	NOP; accepted for backward compatibility.
BBH	4 bytes of data apply on Read/Write Long commands.

5.1.24. Set Multiple Mode—C6H

The Set Multiple Mode command enables the drive to perform Read and Write Multiple operations and establishes the block count for these commands. Currently, max. Multiple count is 1.

5.1.25. Set Sleep Mode- 99H, E6H

These commands put the drive into sleep mode.

5.1.26. SMART- B0H

This command implements the ATA S.M.A.R.T feature set; details are in the S.M.A.R.T section.

5.1.27. Standby, Standby Immediate—96H, E2H, 94H, E0H

The Standby and Standby Immediate commands put the drive into standby mode.

5.1.28. Write Buffer—E8H

The Write Buffer command enables the host to overwrite contents of the drive's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

5.1.29. Write DMA, Write DMA Ext- CAH, CBH, 35H

These commands write a number of sectors as specified in the Sector Count register, using DMA mode transfer.

5.1.30. Write Log Ext- 3FH

This command writes data to the general purpose log of the device. The writable logs are described in the SMART log section.

5.1.31. Write Multiple,Write Multiple Ext Commands—C5H, 39H

The Write Multiple command is similar to the Write Sectors command. The drive sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block that contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

5.1.32. Write Sector(s),Write Sector(s) Ext—30H, 31H, 34H

The Write Sectors command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

5.1.33. Write Verify Sector(s)—3CH

The Write Verify Sector(s) command writes and verifies from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

6. S.M.A.R.T Feature Set

Cactus Technologies® -503 series SSDs supports the following SMART commands, when loaded into the Feature Register:

Value	Command
D0h	SMART read data
D1h	SMART read attribute thresholds
D2h	SMART enable/disable attribute autosave
D5h	SMART read log
D6h	SMART write log
D8h	SMART enable operations

Value	Command
D9h	SMART disable operations
DAh	SMART return status

The following sections describes these commands in detail.

6.1. SMART Enable Operations

This command enables access to the SMART features of the Cactus Technologies® -503 series Industrial SSD devices. For this command to take effect, the following signature bytes must be loaded:

Cylinder Low – 4Fh

Cylinder High - C2h

The state of SMART (enabled/disabled) is preserved across power cycles.

6.2. SMART Disable Operations

This command disables access to the SMART features of the Cactus Technologies® -503 series Industrial SSD devices. For this command to take effect, the following signature bytes must be loaded:

Cylinder Low – 4Fh

Cylinder High – C2h

The state of SMART (enabled/disabled) is preserved across power cycles.

6.3. SMART Enable/Disable Attribute Autosave

For this command to take effect, the following signature bytes must be loaded:

Sector Count – 00h or F1h

Cylinder Low – 4Fh

Cylinder High – C2h

This command is essentially a no-operation as the SMART attribute data is always available and kept current by the device..

6.4. SMART Read Data

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low – 4Fh

Cylinder High – C2h

This command returns one sector of SMART data. The format of the returned data is as follows:

Offset	Value	Description
0 – 1	0010h	SMART structure version
2 – 361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Offline data collection status (no offline data collection)
363	00h	Selftest execution status (selftest completed)
364 – 365	0000h	Total time to complete offline data collection
366	00h	----
367	00h	Offline data collection capability (none)
368 369	0003h	SMART capabilities
370	00h	Error logging capability (none)
371	00h	----
372	00h	Short selftest routine recommended polling time
373	00h	Extended selftest routine recommended polling time
374 – 385	00h	Reserved
386 – 387	0004h	SMART Hyperstone structure version
388 – 391		Firmware commit counter
392 – 395		Firmware wear level threshold
396		Global wear leveling status: '0' – not active, '1' - active
397		Global bad block management status: '0' – not active, '1' - active
398 – 401		Average flash block erase count
402 – 405		Number of flash blocks involved into wear leveling
406 – 409		Number of total ECC errors during firmware initialization
410 – 413		Number of correctable ECC errors during firmware initialization
414 – 510	00h	----
511		Data structure checksum

There are 12 attributes defined for the -503 series products. The following sections describe in detail what these attributes are.

6.4.1. Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks. The data structure of this attribute is as follows:

Offset	Value	Description
0	196	Attribute ID
1 – 2	0003h	Flags – Pre-fail type, attribute is updated during normal operation
3		Attribute value – the value returned here is the percentage of spare blocks remaining summed over all flash chips
4		Attribute value – worse value
5 – 7		Sum of initial number of spare blocks over all flash chips
8 – 10		Sum of current number of spare blocks over all flash chips
11	00h	Reserved

This attribute is used for the SMART Return Status command. If the attribute value is less than a preset threshold determined during at factory low level format process, the SMART Return Status will indicate a threshold exceeded condition.

6.4.2. Spare Block Count Worse Chip Attribute

This attribute gives information about the spare blocks in the flash chip with the lowest current number of spare blocks. The data structure of this attribute is as follows:

Offset	Value	Description
0	213	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – this value is fixed at 100
4	64h	Attribute value – this value is fixed at 100
5 – 7		Initial number of spare blocks in the flash chip with the lowest current number of spare blocks
8 – 10		Current number of spare blocks in the flash chip with the lowest current number of spare blocks
11	00h	Reserved

6.4.3. Erase Count Attribute

This attribute gives information about the number of flash block erases performed. The data structure of this attribute is as follows:

Offset	Value	Description
0	229	Attribute ID
1 – 2	000Xh	Flags – Pre-fail or Advisory type, attribute is updated during normal operation
3		Attribute value – the value returned here is an estimation of the percentage of card life remaining based on the number of flash block erases that have occurred and the target number of erases per flash block.
4		Attribute value – worse value
5 – 10		Estimated total number of block erases
11	00h	Reserved

This attribute is used for the SMART Return Status command. If the attribute value is less than a preset threshold determined during at factory low level format process, the SMART Return Status will indicate a threshold exceeded condition.

The target number of erases is set during factory low level format time. The attribute flag – Pre-fail or Advisory, is also set at that time.

6.4.4. Total ECC Error Attribute

This attribute gives information about the total number of ECC errors on flash read commands. The data structure of this attribute is as follows:

Offset	Value	Description
0	203	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – fixed at 100
5 – 8		Total number of ECC errors, correctable and uncorrectable
9 – 10		--
11	00h	Reserved

6.4.5. Correctable ECC Error Attribute

This attribute gives information about the total number of correctable ECC errors on flash read commands. The data structure of this attribute is as follows:

Offset	Value	Description
0	204	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation

Offset	Value	Description
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – fixed at 100
5 – 8		Total number of correctable ECC errors
9 – 10		--
11	00h	Reserved

6.4.6. UDMA CRC Error Attribute

This attribute gives information about the total number of UDMA CRC errors on flash read commands. The data structure of this attribute is as follows:

Offset	Value	Description
0	199	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – fixed at 100
5 – 8		Total number of UDMA CRC errors
9 – 10		--
11	00h	Reserved

6.4.7. Total Number of Reads Attribute

This attribute gives information about the total number of flash read commands. The data structure of this attribute is as follows:

Offset	Value	Description
0	232	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – fixed at 100
5 – 10		Total number of flash read commands
11	00h	Reserved

6.4.8. Power On Count Attribute

This attribute gives information about the total number of power on cycles. The data structure of this attribute is as follows:

Offset	Value	Description
0	12	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – fixed at 100
5 – 8		Total number of power on cycles
9 – 10		--
11	00h	Reserved

6.4.9. Total LBAs Written Attribute

This attribute gives information about the total amount of data written in units of 32MB. The data structure of this attribute is as follows:

Offset	Value	Description
0	241	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – fixed at 100
5 – 10		Total number of LBAs written, divided by 65536
11	00h	Reserved

6.4.10. Total LBAs Read Attribute

This attribute gives information about the total amount of LBAs read in units of 32MB. The data structure of this attribute is as follows:

Offset	Value	Description
0	242	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100

Offset	Value	Description
4	64h	Attribute value – fixed at 100
5 – 10		Total number of LBAs read, divided by 65536
11	00h	Reserved

6.4.11. Anchor Block Status Attribute

This attribute gives information about the total number time the Anchor block has been re-written, either by a repair operation or by firmware updates. The data structure of this attribute is as follows:

Offset	Value	Description
0	214	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – fixed at 100
5 – 8		Anchor block write count
9 – 10		--
11	00h	Reserved

6.4.12. TRIM Status Attribute

This attribute gives information about the percentage of card capacity that is in trimmed state. The range is from 0 to 99. The data structure of this attribute is as follows:

Offset	Value	Description
0	215	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3		Attribute value
4	01h	Attribute value – fixed at 01h
5 – 10		--
11	00h	Reserved

6.5. SMART Read Attribute Threshold

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low – 4Fh

Cylinder High – C2h

This command returns one sector of SMART attribute thresholds information. The format of the returned data is as follows:

Offset	Value	Description
0 – 1	0010h	SMART structure version
2 – 361		Attribute entries 1 to 30 (12 bytes each)
362 - 379	00h	Reserved
380 - 510	00h	--
511		Data structure checksum

The SMART attribute threshold entries are as follows:

6.5.1. Spare Block Count Attribute Threshold

Offset	Value	Description
0	196	Attribute ID
1		Spare block count attribute threshold defined during low level format
2 - 11	00h	Reserved

6.5.2. Spare Block Count Worst Chip Attribute Threshold

Offset	Value	Description
0	213	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.5.3. Erase Count Attribute Threshold

Offset	Value	Description
0	229	Attribute ID
1		Erase count attribute threshold defined during low level format
2 - 11	00h	Reserved

6.5.4. Total ECC Errors Attribute Threshold

Offset	Value	Description
0	203	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.5.5. Correctable ECC Errors Attribute Threshold

Offset	Value	Description
0	204	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.5.6. UDMA CRC Errors Attribute Threshold

Offset	Value	Description
0	199	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.5.7. Total Number of Reads Attribute Threshold

Offset	Value	Description
0	232	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.5.8. Power On Count Attribute Threshold

Offset	Value	Description
0	12	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.5.9. Total LBA Written Attribute Threshold

Offset	Value	Description
0	241	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.5.10. Total LBA Read Attribute Threshold

Offset	Value	Description
0	242	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.5.11. Anchor Block Status Attribute Threshold

Offset	Value	Description
0	214	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.5.12. TRIM Status Attribute Threshold

Offset	Value	Description
0	215	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

6.6. SMART Return Status

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low – 4Fh

Cylinder High – C2h

This commands checks the health of the device. If either the Spare Block Count or the Erase Count attribute exceeded the factory preset threshold, signature values will be returned in the Cylinder Low/High registers as follows:

Cylinder Low – F4h

Cylinder High – 2Ch

If the thresholds are not exceeded, the Cylinder Low/High registers retains the initially loaded 4Fh/C2h values.

6.7. SMART Read Log

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low – 4Fh

Cylinder High – C2h

This command will return data of the SMART log. The following log addresses are defined:

Address	Description
0x00	Log Directory
0x80 – 0x9F	Host Vendor Specific Logs
0xA0	Reserved
0xA1	Reserved
0xA2	Reserved

The Log Directory at address 0x00 returns one sector of data that shows the number of sectors for Log addresses 1 to 255:

Offset	Value	Description
0 – 1	1	SMART Logging version
256 – 319	16	Number of sectors for Log addresses 0x80 to 0x9F
320 – 511	--	Reserved

6.8. SMART Write Log

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low – 4Fh

Cylinder High – C2h

This command is used to write data to the SMART logs. Only the Host Vendor Specific logs can be written.

Appendix A. Ordering Information

Model KDXFY-503

Where: X is drive capacities:

1G ---------- 1GB
2G ---------- 2GB
4G ---------- 4GB
8G ---------- 8GB
16G ---------- 16GB
32G ---------- 32GB
64G ---------- 64GB
128G ---------- 128GB (*special build; consult factory for availability and lead time*)

Where Y is temperature:
Blank ---------- Standard temperature (0° C to +70° C)
I ---------- Extended temperature (-45° C to +90° C)

Example:

(1) 2GB SSD ---------- KD2GF-503
(2) 1GB SSD Extended Temp ---------- KD1GFI-503

Appendix B.Technical Support Services

B.1.Direct Cactus Technical Support

Email: tech@cactus-tech.com

Appendix C.Cactus Worldwide Sales Offices

Email: sales@cactus-tech.com

US Office:

Cactus USA
3112 Windsor Road , Suite A356
Austin, Texas 78703
Tel: (512) 775 0746
Email: americas@cactus-tech.com

Appendix D.Limited Warranty

I. WARRANTY STATEMENT

Cactus Technologies® warrants its Industrial Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for five years from the date of purchase. This express warranty is extended by Cactus Technologies Limited

II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies® responsibilities regarding the Cactus Technologies® Industrial Grade SSD products. In satisfaction of its obligations hereunder, Cactus Technologies®, at its sole option, will either repair, replace or refund the purchase price of the product.

NOTWITHSTANDING ANYTHING ELSE IN THIS LIMITED WARRANTY OR OTHERWISE, THE EXPRESS WARRANTIES AND OBLIGATIONS OF SELLER AS SET FORTH IN THIS LIMITED WARRANTY, ARE IN LIEU OF, AND BUYER EXPRESSLY WAIVES ALL OTHER OBLIGATIONS, GUARANTIES AND WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR INFRINGEMENT, TOGETHER WITH ANY LIABILITY OF SELLER UNDER ANY CONTRACT, NEGLIGENCE, STRICT LIABILITY OR OTHER LEGAL OR EQUITABLE THEORY FOR LOSS OF USE, REVENUE, OR PROFIT OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION PHYSICAL INJURY OR DEATH, PROPERTY DAMAGE, LOST DATA, OR COSTS OF PROCUREMENT OF SUBSTITUTE GOODS, TECHNOLOGY OR SERVICES. IN NO EVENT SHALL THE SELLER BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, ARISING OUT OF THE USE OR INABILITY TO USE SUCH PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

Cactus Technologies® products are not warranted to operate without failure. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or back-up features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within five years of purchase, Cactus Technologies® will have the option of repairing or replacing the defective product, if the following conditions are met:

A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.
B. An incident drive filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.
C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding storage or maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty shall be tested to the product’s functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs.

Cactus Technologies® reserves the right to repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

Cactus Technologies® may, at its discretion, ship repaired or rebuilt products identified in the same way as new products, provided such drives meet or exceed the same published specifications as new products. Concurrently, Cactus Technologies® also reserves the right to market any products, whether new, repaired, or rebuilt, under different specifications and product designations if such products do not meet the original product's specifications.

IV. RECEIVING WARRANTY SERVICE

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies Limited Please contact Cactus Technologies® Customer Service department with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies® will issue a Return Material Authorization or Product Repair Authorization number and instructions for shipping the product back to us for service.